Large-Area MOVPE Growth for HEMT LSI

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Abstract
We report on metalorganic vapor phase epitaxy (MOVPE) for high electron mobility transistor (HEMT) LSI. The low-pressure barrel reactor can grow twelve 3-inch wafers at a time. It is shown that the grown layers meet the demands for LSI application. We fabricated HEMT devices with gates 0.6 μm long using photolithography, with excellent characteristics. We applied our MOVPE technique to HEMT 64Kb SRAM and obtained a typical address access time of 1.2 ns at a power dissipation of 5.9 W.

1. Introduction
The metalorganic vapor phase epitaxy (MOVPE) is expected to be suitable growth technique for HEMT LSI wafers because of its ability for a large-area growth. We have developed an MOVPE technique which meets the demand for HEMT LSIs. Epitaxial layers for use in HEMT fabrication must meet the following requirements: (1) low density of surface defects, (2) extremely high uniformity of epitaxial layers, (3) superior two-dimensional-electron gas (2DEG) characteristics, and (4) precise and highly reproducible control of layer parameters such as layer thickness, carrier concentration, and AlAs mole fraction.

In this paper we describe an MOVPE technique that meets these requirements and its application to 64Kb SRAM [1].

2. Reactor and Growth Conditions
The reactor and growth conditions are given in detail by Tanaka et al [2]. The low-pressure barrel reactor holds twelve 3-inch wafers (Fig. 1). Wafers are rotated to obtain highly uniform epitaxial layers. The susceptor revolves at 3 rpm around the central axis and has twelve facets, each holding a 3-inch wafer. Each wafer rotates at 12 rpm around the local axis. Each facet is tilted 5 degrees to the vertical.

Figure 2 shows the HEMT LSI structure with double-etching-stopper. The structure consists of eight layers, which requires a heterointerface abruptness of one or two monolayers. Trimethyl-
gallium (TMGa) is used for the GaAs buffer and n-GaAs cap layer to shorten growth time. Triethyl-gallium (TEGa) was used to grow thin n-GaAs layer, which makes the difference in threshold voltages between enhancement- and depletion-mode HEMTs beacause a low growth rate is easily obtained. Trimethylaluminaum (TMAI) and TEGa were used for the n-AIGaAs layers. The group-V gas source is arsine and the n-type dopant is disilane. The reactor pressure was kept at 80 mbar and the growth temperature was 680°C.

![Diagram of HEMT LSI structure with double-etching-stopper](image)

**Fig. 2** HEMT LSI structure with double-etching-stopper

3. Characterization of epitaxial layers

3.1 Surface defects

Surface defects or particles on epitaxial wafers degrade the yield and reliability of HEMT wafers. We measured surface defects using a surface contamination analyzer (Surfscan 4500, Tencor Instruments). The total density of particles larger than 0.24 µm² is 8.0 cm⁻². These values are much smaller than state-of-the-art molecular beam epitaxy (MBE) results (Sonoda et al. [3]). The density of surface defects is not affected by wafer rotation.

3.2 Uniformity of donor concentration and layer thickness

The layer thickness was characterized by Capacitance-voltage (C-V) profile. We estimated layer thickness from the peak in the carrier profile of the uniformly doped n-AlGaAs/n-GaAs structure. From TEM (Transmission Electron Microscopy) measurement, we found a linear relationship between the peak position and the true AlGaAs thickness, enabling us to estimate the uniformity of AlGaAs thickness very conveniently. The donor concentration was also measured using the C-V profile in the conventional way. Figure 3 and 4 show the uniformity of AlGaAs thickness and donor concentration. Uniformity is less than ±1%. The uniformity among the twelve simultaneously grown wafers are also characterized in the same way. Wafer-to-wafer uniformity is ±1% for thickness and ±2% for donor concentration. These values are small enough for LSI application.

![Graph showing variation in layer thickness over 3-inch wafer](image)

**Fig. 3** Variation in layer thickness over 3-inch wafer

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thickness, donor concentration and the AlAs mole fraction, written approximately as

$$V_p = eN_Dd^2/2\varepsilon + \Delta E_c \cdot \Phi_B$$  \hspace{1cm} (2)

where

- $N_D$: AlGaAs donor concentration
- $d$: AlGaAs thickness
- $\varepsilon$: AlGaAs dielectric constant
- $\Phi_B$: Al/AlGaAs Schottky barrier height
- $\Delta E_c$: AlGaAs/GaAs band discontinuity.

Empirical fitting gives the dependence of AlGaAs thickness and donor concentration as

$$V_p = 7.71 \times 10^{-4} N_Dd^2 - 1.07 \hspace{1cm} (V)$$  \hspace{1cm} (3)

($N_D$ in $10^{18}$ cm$^{-3}$ and $d$ is in nanometers).

We can characterize the combined variation of epitaxial layer parameters by measuring $V_p$. The correspondence between $V_p$ from C-V measurement and $V_{th}$ in actual devices depends on the design rule and fabrication process in a very complicated manner. With the design rule and fabrication process fixed, however, we can easily predict the variation in $V_{th}$ due to layer parameter variation without actually having to fabricate the transistors.

Figure 5 shows the variation in $V_p$ with respect to the AlGaAs thickness. Horizontal axis is a nominal thickness calculated from the growth time. The $V_p$ varies according to eq. (3) even with a 0.5 nm variation in thickness. This indicates that thickness control of nearly one atomic layer can be achieved in our reactor.

We routinely grew a standard n-AlGaAs/GaAs structure ($N_D=1.4 \times 10^{18}$ cm$^{-3}$ and $d=47.5$ nm) with the same growth condition and observed the run-to-run fluctuation of $V_p$ over the long term. Figure 6 shows the variation of $V_p$ during eight months. The vertical axis is the run number of the samples. The difference in the maximum and minimum values is 140 mV. If we assume that the thickness and donor
concentration fluctuate independently by ±1%, eq. (3) gives 146 mV variation. This means the run-to-run variation in parameters is less than ±1%.

![Graph](image)

**Fig. 5** Pinch-off voltage variation with AlGaAs thickness

![Graph](image)

**Fig. 6** Variation in pinch-off voltage during 8 months (25 RUNs / month on the average)

4. Application to HEMT 64Kb SRAM

4.1 Fabrication process

For stable and fewer processing steps, we developed a double-etching-stopper process [1]. In this process sequence, the E- (enhancement) and D- (depletion) mode recessed-gate HEMTs are fabricated at the same time. This sequence is based on a selective GaAs dry etching technique using CCl₂F₂ as the etchant gas. The fabrication process is as follows: (a) the GaAs cap layer at the E-mode HEMT region is selectively etched before gate layer lithography is performed; (b) oxygen ions are implanted to isolate device, the SiON layer and AuGe/Au ohmic contact electrode are formed, and the SiON layer is etched through the photoresist pattern of the gate electrode; (c) two recessed-gate etching steps using two n-AlGaAs etching stopper layers are introduced to lower source resistance. The gate electrode is evaporated and lifted-off. This aluminum gate electrode is also used for the first interconnection layer. (d) The second interconnection layer (Ti/Pt/Au) is formed on top of the SiON layer.

Total fabrication for the 64Kb SRAM took 8 photolithography steps, including formation of the surface passivation layer.

4.2 Basic device performance

A 0.6 μm-gate HEMT was fabricated using photolithography instead of electron beam lithography. A transconductance and K-value are 340mS/mm and 690mS/V/mm, respectively. The cut-off frequency was 38 GHz. The uniform epitaxial layer growth technique and double-etching-stopper process made the standard deviations of threshold voltage 11.6 mV for the E-mode and 12.0 mV for D-mode HEMTs. These values are less than 2% of the logic voltage swing for DCFL (Direct Coupled FFET Logic). In a 51-stage ring oscillator, a mean delay time of 22.6 ps/gate is obtained with a 0.8 ps standard deviation over the 3-inch wafer and a power dissipation of 0.8 mW/gate.

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4-3 Design and operation

To reduce access time, the memory cell array is divided into 4Kbx16 memory planes, and a data line equalization technique is introduced. This RAM has two spare rows and columns in each 4Kb plane for redundancy. The I/O interface is ECL-compatible. An E/D-type DCFL is used for the basic logic configuration. Supply voltages are -1.0 V, -2.0 V and -3.6 V. The -1.0 V supply voltage is used for the DCFL gate. An E/D-type source follower buffer is introduced for the word driver circuit. This circuit is normally cut off, if being not selected. In 8Kx8-bit SRAM, 8 word lines are selected from 256, which reduces power dissipation.

Figure 7 shows the fabricated SRAM. The chip size is 7.4 mm x 6.6 mm. Figure 8 shows the address input and data output waveforms at room temperature. A typical address access time of 1.2 ns has been obtained at power dissipations of 5.9 W, including the delay time in the I/O circuit. This power dissipation allows the operation in a normal forced-air cooling environment. A write pulse width of less than 1 ns is available for the SRAM.

Fig. 7 Micrograph of HEMT 64Kb SRAM

![Micrograph of HEMT 64Kb SRAM](image)

5. Summary

We have developed an MOVPE technique for HEMT LSIs. The reactor can grow twelve 3-inch wafers at a time. The uniformity, controllability, reproducibility, and the electrical quality of the epitaxial layers satisfies all the requirements for LSI applications. We applied this technique to HEMT 64 Kb SRAM and demonstrated MOVPE-grown wafers are of LSI-quality.

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Reference