ABSTRACT

The high rate data transfer between CPU and memory in future high performance systems requires the 64 Meg DRAM and generations beyond to take a new design approach. Fast RAS access time together with a wider I/O path are key DRAM performances indices for achieving high bandwidth CPU-MEMORY data operations. In this paper a novel Hierarchical Multi-Datalines (HMD) Architecture with a wide I/O path and high speed circuit design techniques used to implement this architecture in a 64 Meg DRAM are described.

HIERARCHY MULTI-DATALINES ARCHITECTURE

In a traditional high density DRAM, although a large number of memory cells are selected after each RAS cycle, only a small amount of bit data is passed through the sense amplifier banks to the main datalines to reach one or four output buffers. For a wider I/O of eight outputs, or more, DRAM memory devices need an architecture that can support both high speed and multiple datalines configurations. Figure 1 shows the chip diagram for such a 64 Meg DRAM. Peripheral circuits at the middle section of the chip divide the memory array into two 32 Meg arrays along the length of the chip. The Y decoders separate each 32 Meg array into two 16 Meg arrays, and a Wide Data Path Circuit (WDPC) at the center of each 16 Meg array further divides this 16 Meg array into two 8 Meg blocks. Each memory block contains 16 sense amplifier banks separated by 256 wordlines which are driven by row decoders placed between the peripheral circuitry and the memory arrays.

A simplified HMD array structure is shown in figure 2. A Sub I/O pair which runs parallel with the wordlines is configured the same as conventional DRAM design where CMOS latching sense amplifiers (S/A) are connected to I/O lines by N-channel I/O pass gates. However, unlike a conventional DRAM, each Sub I/O pair in this chip is connected to only four S/As. A local differential amplifier, an integral part of high speed direct sensing, is placed in the pitch of four S/As. Two signal lines, YREAD and YWRITE from the Y decoder, control the connections of the Sub I/O pair to the Local I/O lines during read and write operations respectively. These read and write control lines from the Y decoder also control the WDPC circuits which are placed at the end of the Local I/O lines.
The HMD array architecture allows high speed direct sensing of small signals from the bitlines, but without the area penalty of one differential amplifier per S/A as in recent DRAM architectures [1]. The DRAM write and read operation of the HMD scheme are as follows:

During the DRAM write operation the data input from the Main I/O circuit is driven through the WDPC from the input buffer. The YWRITE signal places data onto the selected Local I/O lines and Sub I/O pairs. The S/As are over-driven with data from the Sub I/O lines as gated by the the S/A select signals.

In the DRAM read operation, data from the bitlines travel through the S/A and the Nchannel I/O pass gates to arrive at the input gates of the differential amplifier. The YREAD signal turns on the current source and converts the bitline differential signals to currents flowing through the Local I/O line. Read signals from the Local I/O pair are current sensed by the WDPC and the WDPC output in turn drives the Main I/O lines. These Main I/O signals are further amplified and driven by Global I/O circuits to the output buffers.

In parallel with the WDPC signal propagation, the S/A performs the task of restoring bitline data using the conventional sensing, latching and restoring techniques. Individual N channel pull down transistors at each S/A are employed to improve the sensing accuracy and speed. Matching of the S/A sensing delay to the wordline delay is achieved by similarly loading the S/A control signals and the wordlines. VSS power lines for the sense amplifier banks are meshed throughout the memory array by utilizing wordline strapping areas to reduce the effective resistance of the lines.

There are 256 Local I/O line pairs per 8 Meg memory block. However, only four Local I/O line pairs and their relative circuits are activated during each DRAM cycle. All other signal paths are kept in a precharge state to avoid high current spikes and high active power consumption. This is one advantage of this architecture over the previously reported multi-dataline DRAM designs [2,3].

LONG SIGNAL LINE CIRCUIT CONFIGURATION

Many critical signals, such as address and I/O lines which have to travel almost the entire length of the chip, contribute major fractions of the chip active power and delay. Figure 3 shows the circuit configuration for long signal lines adopted in this 64 Meg DRAM to improve both the power dissipation and switching speed. Signal drivers are complementary circuits which drive differential signal lines from their VDD/2 precharge state to the power supply rails. Receiver circuits placed at interval along the long signal lines convert the pseudo-differential signals to full CMOS signal outputs.

The Nchannel cross couple input stage of the receiver sets the trip point of this circuit equivalent to a separation of the differential signal lines by the magnitude of one Nchannel Vt. The effective trip point of the receiver is therefore Vdd/2 as compared to the VDD/2 trip point of a conventional CMOS inverter.

To avoid hot carrier problems associated with possible over-boostrapping of the wordline driver voltage during normal operation as well as during the accelerated burn-in, the RAM employs an on-chip charge-pump high voltage supply (VPP) regulated at 5.0 V. Figure 4 shows a circuit implementation of this scheme. A hot carrier effect software tool [4] was used to determine the critical circuits that need protection from the hot carrier effects.
The chip uses a 0.4μm double metal CMOS process and a Modified Trench Capacitor cell [5]. The chip size is 23.3mm x 11.5mm and cell size is 1μm x 2.0μm. Table 1 summarized the RAM characteristics. Worst case SPICE simulations show the RAM dissipates 480mW of power and can achieve 40ns RAS access time as shown in figure 5.

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