A 32 Bit Microcontroller with an Embedded Flash EEPROM

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ABSTRACT
The development of a versatile 32 bit microcontroller containing various peripheral functional modules including a 512K bit Flash EEPROM will be described. A modular process approach was employed to integrate high voltage transistors and Flash EEPROM cells into the baseline .8μm twin well double metal CMOS process. A modular circuit design approach was utilized to simplify chip design and to reduce development time.

A microcontroller with an embedded Flash EEPROM offers added flexibility and versatility over one with an embedded EPROM. The Flash EEPROM allows the stored data or program to be updated electrically in-system or on-board without the constraints of UV erasing or one-time-only programming. While a Flash EEPROM offers significant advantages over an EPROM in versatility and over the conventional EEPROM in density, it has the inherent shortcomings of over erase, high erase current, and program disturb problems. These problems can result in reduced operational windows for process parameters, and increased operational constraints including program-before-erase, intelligent write, and limited low VDD capability, that make the Flash EEPROM less than ideal for microcontroller applications. In this development, a new Flash EEPROM cell along with new circuit techniques were developed to overcome these problems.

While logic circuits for microcontrollers operate at a 5V supply, non-volatile memories including the Flash EEPROM involve high voltage circuits of over 12V. Since scaled submicron transistors with a relatively thin gate oxide are not suitable for high voltage operation, special high voltage transistors with a thicker gate oxide were required for high voltage circuits. Also, Flash EEPROM cells require a special double poly floating gate structure with thin tunnel oxide for program and erase. In this development, a modular approach was employed to develop optional process modules that can be selectively integrated into the baseline process without affecting the baseline device characteristics.

Many system applications require an embedded microcontroller with high performance and high functional integration which can only be met by a 32 bit microcontroller. The high complexity of a 32 bit microcontroller required a new design methodology to alleviate complex design and testing, as well as long development time problems. In this development, a modular design approach was adapted for overcoming the limitations and difficulties associated with the 32 bit microcontroller design. This approach subdivided the chip into many functional modules which can be designed and tested independently and simultaneously in parallel.

SCSG FLASH EEPROM CELL
For microcontroller applications, a Flash EEPROM has a different set of priorities from those for a stand alone commodity memory product. Maintaining compatibility with the baseline process, using existing facilities for production, imposing no tighter process parameters windows, maintaining low cost production, realizing noncritical operational timings, and achieving 3V operation capability, are some key factors for a Flash EEPROM for microcontroller applications. The conventional Flash EEPROM cell [1-3] could not meet all these criteria, and therefore, a new SCSG cell was developed.

The new Flash EEPROM cell, dubbed the SCSG (Source Coupled Split Gate) cell, offers many important features that eliminate the shortcomings associated with the conventional cell. The over erase problem is eliminated by incorporating a split gate structure on the source side of the cell. High erase
current is eliminated by a special erasing structure to avoid band to band tunnelling and impact ionization within the tunnel region. The structure has the floating gate coupled to the source to form a tunnel region, in which As implant is made to avoid any junctions. Figure 1 shows a topographical layout of the SCSG cell. The very low erase current for the SCSG cell made practical an on-chip high voltage generator for erasure to reduce erase time and to minimize VPP sensitivity.

Figure 1: The SCSG flash EEPROM cell

Programming of the cell is achieved through channel hot electron injection on the drain side, whereas erasure is achieved through Fowler-Nordheim tunneling on the source side between the floating gate and the substrate. The separate silicon regions for program and for erasure allow process optimizations to be made independently to achieve the best possible performance and to minimize the cell program disturb problem. The SCSG cell utilizes the same thin oxide under the floating gate in the tunnel region and in the channel region. An Oxide/Nitride/Oxide (ONO) stack was used for interpoly dielectrics and for the split gate dielectrics. Figure 2 and Figure 3 show program and erase characteristics, respectively, for a SCSG cell.

Figure 2: SCSG cell programming characteristics

Figure 3: SCSG cell erase characteristics

**PROCESS**

Optional process modules which can be integrated into the baseline process, including a high voltage process module and a Flash EEPROM cell process module, were developed [4]. The baseline process features a .8µm twin-well CMOS technology with double metal for interconnection. Both NMOS and PMOS transistors have a gate oxide of 150Å and a lightly doped drain (LDD) structure.

The high voltage process module contains a double poly structure for capacitors and high voltage PMOS and NMOS transistors. The high voltage transistors use poly 1 gates with a thicker gate oxide of 350Å, as compared to the low voltage transistors. The same LDD process, optimized for the high speed baseline process was utilized for high voltage transistors without modifications. Table 1 compares some key process and device parameters for the baseline low voltage and high voltage devices.

**Table 1: Low voltage and high voltage devices**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Low Voltage</th>
<th>High Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>LDD PMOS and NMOS</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Field Oxide</td>
<td>550Å</td>
<td>5500Å</td>
</tr>
<tr>
<td>Transistor gates</td>
<td>Poly 2</td>
<td>Poly 1</td>
</tr>
<tr>
<td>Gate Oxide Thickness</td>
<td>150Å</td>
<td>350Å</td>
</tr>
<tr>
<td>Vtn</td>
<td>0.85V</td>
<td>0.75V</td>
</tr>
<tr>
<td>Vtp</td>
<td>-1.0V</td>
<td>-0.95V</td>
</tr>
<tr>
<td>Lef</td>
<td>0.6µm</td>
<td>1.6µm</td>
</tr>
<tr>
<td>Field Inversion</td>
<td>&gt;12V</td>
<td>&gt;15V</td>
</tr>
<tr>
<td>Field Punch-Through</td>
<td>&gt;12V</td>
<td>&gt;15V</td>
</tr>
</tbody>
</table>
process and for the optional high voltage process. The ONO stack is used as the interpoly dielectrics and has an effective thickness of 310 Å. The high voltage process module requires four additional photoresist steps over the baseline process.

The Flash EEPROM cell process module provides a double poly floating gate structure with a split gate channel region and a tunneling region. The same ONO stack used in the high voltage process module is also used in the Flash EEPROM cell to form floating gate devices. The ONO stack has an effective thickness of 310 Å between the two poly layers, and 250 Å in the split gate channel region. The same oxidation process is used for growing floating gate oxide in the channel region and in the tunnel region to realize thicknesses of 95 Å and 110 Å, respectively. An implant of As in the substrate tunnel region was made before poly 1 deposition. Three additional photoresist steps, over the combined steps for the baseline and the high voltage process, were required for the Flash EEPROM cell process module.

The modular process approach developed allows the optional process module to be integrated into the baseline process without affecting the baseline transistor characteristics, as the added optional processing steps are confined completely between the isolation and the second gate (low voltage transistor gate) device formation.

**FLASH EEPROM CIRCUIT DESIGN**

Special circuit techniques were developed for the Flash EEPROM design to achieve wide operational margins and high speed performance. The techniques include zener diode regulated programming voltages, a new differential sense amplifier, and internally generated high erasing voltage [5].

Zener diodes were used in generating the drain and the control gate voltages for programming to avoid any unintentional programming of adjacent cells, to achieve optimum program characteristics, and to minimize program disturb. The targeted drain and control gate voltages were 6.5 V and 8.5 V, respectively. The zener diode used, a by-product of the Flash EEPROM cell process, had a breakdown voltage of 7.5 V that is identical to the drain breakdown voltage of the cell. No extra processing steps are required for the diode.

A high sensitivity differential sense amplifier was developed not only to achieve high speed operation but also to minimize any effects from possible cell program disturb and read disturb. Figure 4 shows the new differential sense amplifier circuit. A special current biasing technique was utilized for sensing to eliminate VDD sensitivity and to achieve a consistent biasing for low VDD operation. The bit line voltage is regulated to be under 1.0 V to eliminate any possible read disturb.

![Figure 4: A new differential sense amplifier](image)

The high voltage generator for erase operation is a single stage charge pump circuit that achieves a high voltage of near 14 V. The charge pump generator eliminated the VPP supply sensitivity and elevated the erase voltage over that of the supply voltage to reduce erase times.

The Flash EEPROM module was designed to accept variable array sizes ranging from 64K bits to 512K bits in a minimum of 32K bits increment. Prevention of unintentional program or erase of the array was accomplished by a prescribed operational sequence of register writes that had to be properly executed before any program or erase operation could take place. Bulk array stress tests were implemented for production test time reduction. The Flash EEPROM module can also be programmed to serve as a bootstrap ROM during power up, and as an emulator for an external ROM during system development.

**CHIP DESIGN**

The modular design approach subdivided the complex 32 bit microcontroller into separate functional blocks, including CPU, timer, memories, serial communication, analog to digital converter, chip select and system integration etc., which can be designed and tested as independent modules. Functional modules on chip are interconnected physically through an inter-module bus (IMB), and functionally through
the on-chip system integration module (SIM). The interface between a functional module and the IMB followed predefined timings and loading characteristics. All functional modules were designed to have a predetermined height for placement compatibility.

The modular approach achieved high portability for a functional module through the available design database and test vectors. The approach simplified significantly the design task for a complex chip, and can also reduce significantly the design cycle time for a new microcontroller containing either only pre-existing functional modules or both pre-existing and new modules. The approach also proved to be very effective and efficient for new technology and new module development. In this development, a newly designed 256Kb Flash EEPROM module was placed into a proven microcontroller [6] with a minimum effort to generate a mask set for process development and for design verification. Figure 5 shows a die photo of the developmental chip. The proven Flash EEPROM design was implemented into a new 32 bit microcontroller shown as a plot in Figure 6.

Figure 5: A microphotograph of the developmental 32 bit microcontroller

The new 32 bit microcontroller has been designed using the modular approach developed. The new microcontroller contains several peripheral modules in addition to the CPU and 512K bits of Flash EEPROM. The chip contains a total of over one and a half million transistors and has a chip area of 97 square millimeters using the current 0.8µm technology. The chip was designed so that it can be shrunk in the future, without design changes, for technology of 0.6µm and below.

RESULTS

The initial 32 bit microcontroller that contained the new 256K Flash EEPROM module was used as a development vehicle for Flash EEPROM process development and for Flash EEPROM module design verification. Wafers for the chip were processed and devices were characterized. Special emphasis was placed on new Flash EEPROM module characterization and on process compatibility evaluation for the pre-existing modules. Successful development of the process modules and integration of these modules were fully demonstrated from fully functional chips and modules produced and characterized.

The microcontroller including the 256Kb Flash EEPROM module was functional at a system clock frequency of over 30MHz at 4.5V and room temperature. Typical array program time is 20us and erase time is 5 sec which is expected to be reduced to less than 1 sec through internal charge pump and cell layout optimization implemented in the new 32 bit microcontroller chip. Effectiveness of the internal charge pump in reducing the VPP effect on erase time is shown in Figure 7. Programming time as a function of the supply voltage VPP is shown in Figure 8. The 256Kb developmental module demonstrated an endurance of well over 10K program/erase cycles, with no changes in erase times and less than 40% increase in program time after 10K cycles.

An extensive characterization on program disturb showed the minimum program disturb time to be over 10s, which is more than two orders higher than the minimum number required for a 512Kb cell array. Characterization
results also showed no detectable programming effects on erase times, and only a small erasing effect on program times (less than 10μs increase in programming times for greatly over erased cells).

![Figure 7: 256Kb flash EEPROM erase time as a function of VPP](image)

![Figure 8: 256Kb flash EEPROM programming time as a function of VPP](image)

With no program disturb and no over erase problems observed, the developed Flash EEPROM can be programmed or erased based on predetermined time limits without relying on intelligent program, program before erase, and intelligent erase, typically required to avoid serious over erase and program disturb problems.

**CONCLUSION**

A new 32 bit microcontroller with an embedded Flash EEPROM module has been successfully developed using a modular approach for both process and chip design. Many problems associated with the conventional Flash EEPROM cell have been overcome by new cell and circuit techniques developed, to achieve ease of operation and high manufacturability.

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**REFERENCES**