DOUBLE SPACER TECHNIQUE FOR TITANIUM SELF-ALIGNED SILICIDATION TECHNOLOGY

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Abstract
Besides the conventional sidewall oxide spacer used in Titanium Self-Aligned Silicide process, an additional pair of sidewall spacer was applied to extend the distance of silicidated gate and the source/drain region. Junction integrity and bridging problem between the gate and source/drain can be improved by this additional spacer.

Introduction
As the device dimension is further reduced to sub-micron level, the optimization of device design and periphery technology becomes more critical. Lightly doped drain (LDD) structure is one of the most famous design to reduce the hot electron effect, and in some case, is also combined with metal (typically titanium or cobalt) silicidation technology to reduce periphery resistance. The trade-off between spacer length for device design and lateral encroachment of silicidation process makes the conventional salicide process more difficult.

In the application of the salicide process, there are several issues are concerned, such as reaction of Ti/Si, SiO, thermal stability of silicide[2,3], junction leakage[4,5] and gate to source/drain bridging [6-9]. For the bridging problem, there are several approaches, such as TiN formation on top of Ti, Molybdenum capped[6], TiW or W capped[7], oxide or nitride capped[8] and alpha-Si/Molybdenum capped[9] process to reduce lateral growth of TiSi during the silicidation process. This paper discloses another approach to further improve the junction integrity and bridging problem.

Experimental Procedures
Table 1 shows the process procedure of CMOS device with double spacer self-aligned technique. Typically, the gate oxide thickness is 25nm and N+, P+ junction depth are 300nm and 350nm respectively. After the definition of lightly doped drain (LDD) structure was defined by using the first oxide sidewall, an additional low pressure oxide with thickness of 350nm was deposited onto the entire surface of the wafer. Then, anisotropic etching using freon gas and oxygen plasma technique was used to etch away the oxide layer, leaving another sidewall spacer to extend the spacer length. Prior to the deposition of titanium, the wafer was cleaned. Atmosphere furnace with titanium control wafer[3] was used to perform the silicidation process.

The two step annealing silicidation process was performed using N as reaction gas. The temperature of the following flow/reflow process was performed at 850 degree centigrade to remain the thermal stability of silicide films. Junction leakage was tested by using HP4140B meter at a reverse voltage of 7 volts, and the failure criteria was defined to be 100pA. For the testing of bridging, current between the silicided gate and source/drain stripper with length of 50um. Finally, the input electrostatic discharge protection pattern with field oxide MOSFET and output ESD protection pattern with thin oxide MOSFET design were tested to study the effect of spacer length and titanium thickness.

Results and Discussion
Table 1 shows the process sequence of double spacer salicide (DSS) technique. The second spacer was performed by deposition and
anisotropic etching of low temperature oxide (LTO) after the definition of conventional LDD CMOS process. Figure 1 shows the final structure of MOS device with double spacer salicided gate and source/drain regions. With the formation of second spacer, the silicided gate and source/drain regions can be further extended. As Amano[4] has shown, the Shottky behavior near the bird's beak edge or due to the unsuitable design of titanium thickness and junction depth will induce drastic leakage. In order to make sure no oxide will be remained on the silicon open area, cleaning of the wafer prior to the deposition of titanium should be treated carefully. Figure 2 shows the leakage comparison of N+, P+ junction with field implantation and channel implantation structure. For the field implantation junction, which without any poly gate stripe on the active region, the improvement is not significant. Otherwise, for the junction with channel region, the junction leakage will be improved due to the use of second spacer. Figure 3 shows the improvement of bridging problem of gate and source/drain by using the second spacer. Significant improvement can be obtained due to the introduction of second spacer. During the formation of titanium silicide, the lateral encroachment of Tsi, will induce the shortening of the gate and source/drain. The extension of the spacer due to the second spacer will enlarge the distance between the gate and the source/drain and also reduce the possibility of bridging. As the thickness of titanium is increased up to 70nm, the performance will be reduced. If the thickness of titanium is increased, the surface roughness of silicide area will increase as shown in Figure 4. We observed that the roughness is related to the Electrostatic Discharge (ESD) protection for the silicide device. Figure 5 shows the input and output ESD protection voltage versus titanium thickness. For the ESD protection of device with silicide process, we observed no difference between the single spacer and double spacer.

Summary

A pair of second spacer was used to extend the distance between the titanium silicide gate and source/drain. Junction integrity and gate to source/drain bridging problems can be improved by using an pair of second spacer onto the first spacer for the conventional self-aligned silicidation process. Surface roughness of the silicided region becomes the major killer of the ESD protection ability.

References


Fig.1 SEM cross sectional view of Ti double spacer salicide (DSS) NMOS device with LDD structure
POLY GATE PATTERN AND ETCH. REACHTHROUGH IMPLANT TO FORM LIGHTLY DOPED DRAIN EXTENSION
SIDEWALL OXIDE DEP AND ETCH. S/D IMPLANT AND ANNEAL

(A) S/D OXIDE SIDEWALL OXIDE REACHTHROUGH

OXYDE DEPOSITION
NITRIDE DEPOSITION

(B) OXIDE NITRIDE

DRY ETCHING

SPACER 2 GATE SIDEWALL OXIDE

HF DEGLAZE
SPUTTER DEPOSITION OF TITANIUM

(D) Ti SI/Si TITANIUM/SILICON REACTION
TITANIUM NITRIDE STRIP
ANNEAL

(E) TiSi2

Table. 1 Double spacer salicide process.

Fig. 2 Junction yield improvement of Ti salicide process by second spacer with thickness of 3500Å.

Fig. 3 Improvement of gate and source/drain bridging versus Ti thickness by second spacer. a. first spacer 3500Å, second spacer 3500Å b. first spacer 1500Å, second spacer 3500Å c. Ti thickness 500Å, second spacer 3500Å
Fig. 4 Photograph of Ti silicide surface roughness. a. Ti thickness 300A b. Ti thickness 500A c. Ti thickness 700A

Fig. 5 ESD protection of Ti silicide device

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