E1. (Invited)

APPROACHES TO HIGH PIN COUNT AND HIGH POWER SURFACE MOUNT PACKAGES

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ABSTRACT

Recent VLSI devices for consumer product require packages with high pin count (more than 200 I/Os) and/or high power dissipation (over two watts) capability. This paper will review various approaches to address these requirements with emphasis on surface mount packages. Furthermore, for portable consumer products such as digital cellular telephones, notebook computers or video cameras, thin and light packages will be preferred. Plastic pad array carrier (PAC) will also be described in order to achieve high frequency SMTs.

INTRODUCTION

In view of the progress of VLSI technology in recent years, IC designers will be able to integrate many functions on a single chip by using millions of submicron devices. These VLSI chips often require high pin count packages, more than 200 I/Os, and dissipate high power, over two watts. If these devices are being used in portable consumer products such as digital cellular telephones, pagers and notebook computers, low profile, light weight, surface mount packages will be preferred.

In the past, most semiconductor companies worldwide have invested heavily in the design and wafer processing capabilities of VLSI devices while ignoring the packaging and assembly technologies. Thus, the performance of electrical signals and products will soon be limited by packaging or interconnect delays rather than by the VLSI device itself. Just like everything else, the total system is only as strong as its weakest link.

The capital investment for submicron front end wafer facilities has been sky rocketing; today easily over 500 million U.S. dollars for the eight (8) inch wafer BiCMOS line. From a business point of view, money invested on packaging technology will yield a better return on investment (ROI) than that of silicon front end technology, especially if one uses advanced package technology to leverage an increase in market share. It will be wise to switch our emphasis to packaging and interconnect technologies.

EVOLUTION OF PACKAGES WITH INCREASING INTERCONNECT DENSITY

The trend of increasing I/O pin counts and the requirement to reduce interconnect delays, have forced the evolution of package configuration as illustrated in Figure 1. Dual-In-Line packages have been and are still being used as one of the industry standard packages. DIP is a mature package and is low cost driven by the sheer volume and will remain available for many years. However, the maximum pin count of DIP has been limited to sixty-four (64) leads with the standard 100 mil pitch, even with Shrink DIP lead pitch of 70 mils, 64 leads is the limit. Since the leads of DIP packages are inserted in thru holes on a P.C. board, the lead pitch is actually limited by the spacing of thru hole drilling rather than package design. In order to eliminate the requirement of thru holes on a P.C. board, SMT packages were introduced with various shaped lead forming such as gull wing, butt joints and J leads. Notice that lead pitch for all SMT packages have been reduced to 50 mils or less. At the same time, to replace the wave solder process of thru hole leads, solder paste reflow techniques by vapor phase and I.R. furnace have been introduced for SMT board mounting. Lead arrangements have evolved from the two sided...
rectangular body DIP or SOIC into four sided square body PLCC and QFP style packages. But, for a given package body size, lead counts can be increased only by reducing the lead pitch spacing or using an array terminal concept. Figure 2 tabulates the joint JEDEC/EIAJ proposed high pin count QFP configurations with respect to different body sizes and lead pitch.

Lead counts increase by a reduction of lead spacing, to as low as 0.5mm in today's market. Fine pitch QFP packages impose stringent requirements on manufacturing processes of the package suppliers, pick and place equipment and fine pitch solder paste screening. In order to enhance the handling capability of Fine pitch QFP, improve the coplanarity and protect the integrity of delicate fine leads, the Molded Carrier Ring concept was proposed and has been registered in JEDEC/EIAJ for a family of rings and packages (Figure 3 & 4). The mechanical integrity and reliability of 208 QFP with 0.5mm pitch solder joints have been modeled and experimentally verified by Hewlett Packard and Motorola². Process development work of 0.3mm pitch has been reported by Mashushita³. By using tape automatic bonding (TAB) on inner lead bonding (ILB), TapePak® molded carrier ring can offer lead count up to five hundred leads and above in the future. It is quite obvious that many engineering details must be solved before one can achieve a high yielding, six sigma, Fine pitch QFP production process.

In terms of array terminal arrangement, one can use short pin grid array (PGA) and pad array carriers (PAC) with solder balls for surface mounting, Figure 5. Since both the short pins and solder balls are attached below a rigid package body, PGA or PAC offers a much better handling capability than Fine pitch QFP. Furthermore, PAC offers a very desirable self alignment feature during the board mounting process due to the surface tension of molten solder balls. High I/O PAC's can be used on high density boards and substrates with excellent yields, Figure 6. To ensure the desired fatigue life of solder joints, one has to match the coefficient of thermal expansion (CTE) of package body material with the P.C. board or substrate. For surface mount ceramic PGA or PAC body, ceramic or copper-invar-copper constrained substrates and boards must be used.

THERMAL POWER DISSIPATION CONSIDERATIONS

As the extent of circuit integration and the speed or frequency of the device increases, so will the power generated by the I.C. device. Generally speaking, the power is proportional to capacitance, frequency, number of gates and the square of voltage.

\[ \text{Power} = K \cdot C \cdot f \cdot N_g \cdot V^2 \]

Ideally, the power dissipation issue should be addressed from a total system point of view. From a package and board interconnection point of view, one must design the signal path as short as possible with a low dielectric constant material in order to minimize the resistance, capacitance and inductance. From a circuit and device layout point of view, one should design I.C.'s with low voltage and low power consumption and match the output drivers for the proper lead capacitance.

For a given I.C. device, the package designer has two approaches to improve the thermal characteristics. They are:

A. Internal Heat Spreader and/or External Attached Heat Exchanger

Motorola uses copper heat spreader attached to the die attach pad for Bipolar ECLIPS® devices in plastic PLCC packages, Figure 7. Since the heat spreader and wirebonded device are surrounded by molded plastic, the outside package body outline is exactly the same as a conventional PLCC. However, the plastic mold compound has a lower thermal conductivity than the metal components of the package. To further enhance the thermal path, by reduction in the junction to case thermal resistance, Micro-Cool® was developed. For this configuration, the die is attached to a copper pedestal directly exposed to the package surface as shown in Figure 8. The thermal characteristics for Micro-Cool® packages have been simulated and compared to actual Oja measurements for various air flow conditions, Figure 9. To improve the thermal path and for external heat exchanger attachment, the device...
must be assembled in a die cavity down configuration. Figure 10 illustrates a bipolar ECL gate array device assembled in plastic PGA, cavity down and a huge metal heat sink attached. This package is capable of handling a device up to 20 watts with forced air cooling.

B. Package Body Built Using Improved Thermally Conductive Materials

Aluminum nitride can be used to build the ceramic package body instead of the usual 92 or 96 percent alumina oxide. Thus ten times the thermal improvement, 200 vs. 20 watt/M°C respectively. Therefore, many fine pitch multilayer surface mount PGAs have been made with aluminum nitride on ceramic substrate for super computer application. The good thermal conductivity properties of AIN is used to dissipate heat for high power devices as well as to improve the ease of module replacement during repair or rework. Yet another approach is to use a metal base and cap in M-Quad® as developed by Olin, Figure 11. Since M-Quad® is a cavity package using copper alloy leadframe, it has a lower capacitance and lower inductance than that of plastic QFP using A42 leadframe and molded body.

In general, package designers can optimize and reduce the thermal resistance of device junction to package case, Ojc. But, one has to work with system package engineers in order to lower case to ambient temperature by using the proper air flow or attaching a cooling plate.

THIN PACKAGES FOR PORTABLE CONSUMER PRODUCTS

Recent portable consumer products, such as digital pagers, cellular telephones, and notebook computers require thin, light and low cost surface mount packages. For these applications, we have developed overmolded plastic pad array carriers (OMPAC) as shown in Figure 12. This package consists of a chip, wire bonded to a thin P.C. board and plastic compound transfer molded on only one side of the board. An array of small solder balls are attached on the other side of the P.C. board for surface mount terminals. Total package height can be kept to below 70 mils. The exact pitch and solder ball height will be varied according to the number of total terminals required.

Since the OMPAC is an array format, the total package area will be smaller than fine pitch QFP as illustrated in Figure 13. OMPAC offers excellent manufacturability due to its unique structure. The advantages are:

1. No fine pitch lead damage or coplanarity problems.
2. No fine pitch solder paste screening required.
3. Self aligning feature during board mounting reflow.

We consider the OMPAC SMT assembly is a true six sigma process with high yield and cost effective approach for consumer products. The only negative aspect of OMPAC is its thermal power limitation. Several proprietary improvements have been made such as thermal vias and dummy solder pads in order to achieve an Oja less than 35°C/watt on relatively small, 68 array solder ball OMPAC. The same technology can be applied to build multichip packages or smart card modules. Another question often raised about Pad Array Carrier is the inspectability of solder joints. The answer is very simple. One does not use inspection to build quality parts. X-rays, fiber optics and destructive engineering methods can be used to define, characterize and monitor the processing of solder ball joining, but, one will not be able to screen the PAC products by inspection techniques.

From an electrical performance point of view, OMPAC offers the best characteristics in terms of RCL (resistance, capacitance and inductance). Because of its smaller package size, the shorter signal line traces, the low dielectric constant of the P.C. board substrate, OMPAC was found to have minimal propagation delays and simultaneous switching noise as compared to PGA or QFP packages. Figure 14 lists typical OMPAC electrical characteristics using a single layer, double sided P.C. board substrate. If one uses flip chip in place of wire bonding interconnections on OMPAC, we believe inductance can be kept below two nano henries for all terminals. This performance can not be achieved by any other packaging type, assuming a reasonable cost target.

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In conclusion, progress on the VLSI silicon technology has progressed to the extent that packaging interconnections have become a major limiting factor in overall system performance. Thus, a packaging technology breakthrough is needed in order to fully enjoy the benefits of VLSI in consumer products.

REFERENCES

1. EIAJ General Rules Guard Ring Quad Flat Packages (GQFP), EIAJ ED-7414, November, 1989.

JEDEC Registration TapePak Molded Carrier Ring Family, MO-094-Rev B., October 1990.


E.C.I.P.S. (Emitter-Coupled Logic in Picoseconds)
Figure 9

Figure 10

Figure 11

24 ld SOJ Thermal Resistance Junction to Ambient
Forced Convection linear ft/minute

<table>
<thead>
<tr>
<th>Pin Count</th>
<th>Board Area (in.²)</th>
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<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>100</td>
<td>3</td>
</tr>
<tr>
<td>200</td>
<td>5</td>
</tr>
<tr>
<td>300</td>
<td>7</td>
</tr>
<tr>
<td>400</td>
<td>9</td>
</tr>
<tr>
<td>500</td>
<td>11</td>
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</table>

**Table:**

<table>
<thead>
<tr>
<th>LEAD #</th>
<th>INDUCTANCE (pH)</th>
<th>REMARKS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3.73</td>
<td>Modelling lead is 1.4mil</td>
</tr>
<tr>
<td>2</td>
<td>3.41</td>
<td>Modelling lead is 1.6mil</td>
</tr>
<tr>
<td>3</td>
<td>3.30</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>3.28</td>
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</tr>
<tr>
<td>5</td>
<td>3.15</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>3.09</td>
<td>One of the shortest leads</td>
</tr>
<tr>
<td>7</td>
<td>3.03</td>
<td>One of the longest leads</td>
</tr>
<tr>
<td>8</td>
<td>2.99</td>
<td>Vg lead</td>
</tr>
<tr>
<td>9</td>
<td>2.93</td>
<td>Vn lead</td>
</tr>
</tbody>
</table>

* Package lead cannot be modeled as a single inductor.

**Figure 14:**

MOTOROLA INC. MMTD-APDPL. Project Engineering.

OMPAC-Overlaped Pad Array Carrier

**Figure 12:**

**Figure 13:**

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