A single chip mixed digital/analog signal processor in 1.2 μ CMOS interfacing 4 analog subscriber lines to the PCM digital System 12 exchange

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1. **Abstract**

For the development of a new generation line circuit a 4 channel speech processor was designed and fabricated in a 1.2 μ CMOS technology. The circuit includes digital signal processing for receive and transmit signals as well as the analog frontend interfacing four subscriber lines to a PCM digital exchange. The device is operating on a single 5 V power supply.

2. **INTRODUCTION**

The new trend in subscriber line codecs is to multiplex the digital signal processor over several channels. To decide on the number of channels to be multiplexed 4 major issues are considered: the space and routing on the printed circuit board, the number of pins per package 44 pins max., the die area and the maximum available system clock frequency in the System 12 rack on the connector of the line board: 4 MHz.

From these arguments an optimum compromise was decided for: multiplex 4 speech channels per codec. This architecture allows for a 1 MHz PDM A/D to be down sampled after a single decimator filter operating at 4 MHz taking the four channels in a multiplexed schedule, without introducing any differential group delay.

The same approach is applied for the 8th order receive and transmit high and lowpass filters also including the gain control function of the codec.

To speed up the development, the classical full custom approach was abandoned for the use of module generators and reusable cells. For this purpose upgradable LSI module generators are used adapting the existing CMOS library of building blocks to scaled down technology layout rules. In order to obtain an accurate behavioural model of the used building blocks, a detailed analysis of the simulation views took most of the design effort.

The four channel DSP including the analog front ends is fabricated on a 40 mm² 1.2 μ CMOS die area.

The DSP functions, the RX and TX filters, the decimator, the interpolator and the A/l law transcoder are included as independent data paths, one for the TX and RX filters, one for the decimator and another for the interpolator, the digital sigma delta modulator and the transcoder.

The on chip analog front end contains a Notch filter to cancel the 12/16 kHz payphone signal, a switched capacitor PDM A/D and D/A converter and smoothing filters. The signal to distortion is measured to be 33 dB at -45 dBm for -7 db gain setting.

3. **GENERAL ARCHITECTURE**

a) **TX channels**

To interface the analog RX and TX signals of the 4-channel codec with the 4 SLIC's we have the 4 analog front ends.

On the TX side the signal transmitted by the phone set is buffered by an inverting stage with external input and feedback resistor for two reasons: to have the resistors external is a flexibility to adapt the TX gain over a wide range to be conform with extreme country options but in addition to this we have the digital software selectable gain settings and secondly the inverting input buffer avoids a large common mode input range as the opamp is operating on a single 5 V supply. The input buffer also provides a single ended to balanced conversion, because the rest of the TX path is a balanced circuit. A coars echo cancellation is also accessible by a resistive balance from RX out to TX in.

The second stage of the TX path is a second order anti alias filter in a butterworth configuration to avoid noise folding in the following stage, being a switched capacitor notch filter operating at 1 MHz. This notch filter can operate in a 12 kHz and a 16 kHz mode for different country options. The notch is providing 40 dB attenuation on the 12 kHz or 16 kHz software selectable
metering tone frequency and also has a gain of 10 dB expanding the TX signal as the range becomes available after notching the metering tone away.

The signal, free of switching tones is then driven to the sigma delta A/D converter, a second order sigma delta modulator providing the speech in a 1 MHz PDM code.

Four of these TX front ends in parallel feed their 4 x 1 MHz PDM receive signals into the decimator.

The decimator is basically an FIR filter, as described further in this paper, low passing the high frequency noise generated by the noise shaping spectrum of the sigma delta A/D. The decimator is sampling down the 1 MHz PDM to 32 kHz 16 bit.

The digital hybrid then cancels the echo further down in a 4 taps hybrid filter.

Next in the TX-chain the filters, explained in more detail later in this paper, filter the speech spectrum down to the 4 kHz bandwidth of the PCM channel and implement a software settable gain fine tuning. Finally, before the signal is fed into the PCM channel a selectable A/μ low transcoder provides the logarithmic companding of the voice signal dynamic range.

b) RX channels

In the 4 RX channels you recognize the 5 building blocks performing symmetrical functions as compared to the TX path.

Coming from the PCM channel the A/μ Law transcoder is decompressing the voice data and feeding the result into the filters where we also provide the software settable gain coefficient. In the filters the sample frequency of the voice data is up-converted to 32 kHz. In the next stage, the interpolator, the sample frequency is further increased up to 256 kHz by linear interpolation before the second order digital sigma delta modulator converts the 16 bit voice into 2 MHz PDM. The 2 MHz PDM sample frequency is mandatory to be able to meet the target of -90 dBm idle noise.

In the analog front end the 2 MHz RX-signal is converted into a balanced voice signal by a sigma delta D/A converter and low passed by a second order smoothing filter before it is buffered into the RX output.

4. CONCLUSIONS

A 4 channel codec, including the analog frontends, meeting the CCITT requirements is described in this paper.

It has been shown that, although there is no large benefit of area reduction in the analog part, integration of different analog channels together with large digital signal processing power can meet the high standards of channel isolation on the same substrate.

The combination of digital processing together with PA modulation techniques and carefully designed analog blocks gives an outstanding performance in the 4 kHz speech band.

References:


3) V. Friedman, "A dual-channel sigma delta voiceband PCM codec", IEEE 1988 custom integrated circuits conference.


GENERAL ARCHITECTURE

PHOTOGRAPH OF THE 40 W² DEVICE

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