A 13-BIT ANALOG INTERFACE FOR MICROPROCESSOR-BASED SYSTEMS

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Abstract

The following paper describes an integrated data-acquisition system designed as a microprocessor peripheral. The analog functions are centered around a 13-bit self-calibrating analog-to-digital converter and a bandgap reference. The digital section holds a sequencer and a FIFO in order to reduce the number of interrupts presented to the CPU while the chip is scanning automatically up to 8 analog inputs. Special design techniques are described to reduce the injection of digital noise during conversion and to preserve the accuracy of the analog section inside a high speed digital environment.

Introduction

Microprocessor-based systems are running with ever faster clocks while they still have to communicate with the analog world at the same pace. Reading data out of sensors has always been a burden to the CPU and required dedicated circuitry to interface with the comparatively slow A/D converters. While microprocessors are now running at 25MHz and more, typical high performance converters need several microseconds to complete a conversion. This paper will describe an integrated data-acquisition system which solves this problem while maintaining its accuracy in a high speed digital system environment with a single 5V power supply.

Analog section

The heart of this data-acquisition chip is a self-calibrating 12-bit sign A/D converter with fully differential input signals and reference signals. Powered with a single 5V supply to be compatible with digital systems, each analog input voltage can only swing from 0V to 5V but the difference between the 2 input voltages will swing from -5V to +5V maximum. The converter will work over this range, extracting the sign bit first. It also accepts a common-mode input range (the average of the 2 input voltages) from 0 to 5V. The converter uses charge redistribution with capacitor arrays: one main array for conversion, one array for offset calibration and correction and one array for calibrating and correcting the linearity of the main array [1]. The whole circuit is fully differential as shown in figure 1.

Figure 1: A/D block diagram

The self-calibration is performed under the user control and lasts about 1 ms. During the self-calibration sequence, the comparator offset and the 13 capacitor calibrations are automatically performed 8 times at a slower pace than the regular conversion. Using an A/D, the 14 correction coefficients are averaged and then stored in an internal RAM. During conversion, the coefficients are read and the corrections are applied appropriately on the offset and capacitor correction arrays. In order to accommodate the full input range for the input voltages and the reference voltage while preserving the rejection of the capacitor 1st order voltage coefficient, an input common-mode generator is used [2]. An averaging sample-and-hold samples the input signal at the beginning of the acquisition and the resulting voltage is applied to pre-charge the top plate of the capacitor arrays. Such a self-calibrating scheme allows to preserve the full accuracy of the A/D converter over temperature and over time. Figure 2A shows the linearity of the A/D converter before running the calibration with a large offset and...
full-scale error as well as large differential non-linearities. Figure 2B shows the same part after calibration.

The converter can be operated in 3 different modes:
- a 13-bit mode (12 bit + sign) performed with correction in 8.6us,
- a 9-bit mode (8 bit + sign) in 4us,
- a "watchdog" mode where the analog input is compared to 2 digital limits in 1.6us.

An analog multiplexer in front of the A/D selects 2 out of the 8 analog inputs or ground thus forming any combination of fully differential or single-ended inputs. A 2.5v bandgap reference is also provided for generating the reference inputs or as a virtual ground for external analog circuits working with a single 5v supply.

In order to accommodate all the possible modes of conversion and all the possible analog inputs, an instruction RAM can be loaded with up to 8 instructions which are executed sequentially. Each instruction calls for 2 inputs from the multiplexer, an acquisition delay for adapting to various input impedances, the mode of conversion and the use of a timer to slow down the conversion rate if needed. When the watchdog mode is selected, the instruction also holds the 2 digital limits. Once the sequencer is started, each instruction is executed and the result of every conversion is stored into a 32 bit FIFO with the instruction address tag. During the execution, conversions are immediately started at the next internal clock edge after a programmable acquisition delay or they can be synchronized with an external signal brought through a dedicated pin. A complete set of 8 maskable interrupts is provided to communicate with the CPU and a status register gives information on these interrupts and on all activities inside the chip such as the number of data stored in the FIFO, the actual instruction being executed or the alarms detected during watchdog operations. One of the interrupt flags signals when the chip power supply goes below 4v, warning the system that the last conversion results might have been corrupted. The CPU controls the chip by writing into a configuration register: start/stop, reset, perform calibration and power-down. The A/D converter calibrations are performed under the CPU control by writing into this configuration register.

Digital section

Centered around the A/D converter, a block diagram of the whole chip is shown in figure 3.

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register: it is sufficient to calibrate the capacitators only once after power-up since the matching of the array is not sensitive to external conditions, but the offset calibration can be performed once or at every conversions for systems where the supply voltage variation or the temperature variation is large. All registers and memories are directly accessible by the microprocessor which sees them as a memory location. They are all 16 bit wide and are linked by an internal data bus. The chip can interface to either 8-bit or 16-bit external data bus and the access time through the 16-bit bus is typically 30ns, allowing access by most microprocessors without inserting wait states. For an even faster and transparent access, a DMA channel is provided in order to down-load the chip FIFO directly into the system memory.

Noise considerations

Preserving the accuracy of the analog circuitry inside noisy high speed digital systems required several steps to be taken. First, a fully differential structure was chosen for all analog circuits, at the expense of doubling the required hardware. The benefits are the doubling of the dynamic range and the conversion of most of the injected digital noise (through the power supply, the substrate,...) into common mode noise. This type of noise is attenuated by the Common Mode Rejection Ratio (CMRR) of the analog circuits which is typically higher than 60dB. The second step was the averaging of the calibration, performed at a clock rate slower than the one used during conversion, in order to reject the noise generated inside the analog block. A circuitry was also added to stop the internal clock whenever the chip is accessed by sensing the chip select signal (figure 4).

![Clock Removal Circuit](image)

Figure 4: Clock removal circuit

Each time the chip select signal is pulled high by the CPU, the following clock pulses are removed and the whole A/D converter which runs with this clock, is frozen until the chip select is brought back low. Since the largest contributors of digital noise are the internal I/O buffers driving the microprocessor data bus and generating large current spikes when switching, by stopping the clock all critical analog decisions are postponed until the buffers are back to high impedance state. This also helps to synchronize the access to the registers, RAM and FIFO.

As it can be seen on the chip photomicrograph, the layout has been partitioned into physically separate analog and digital sections with separate power and ground pins and wide power and ground bus.

![Chip Photomicrograph](image)

Figure 5: chip photomicrograph

Implementation

The chip was designed using a 1.5μ CMOS digital process (2 metal layers) with an extra mask for generating capacitators. The layout of the digital section has been automatically generated using a standard cell library but the layout of the analog section with the self-calibration logic has been carefully handcrafted. The die area is 5.2 x 4.3 mm2 consisting of 30,000 transistors and the power consumption is 25mW active and 50μW in stand-by. Due to the self-calibration, the part is packaged in a plastic chip carrier (PLCC) and does not suffer from accuracy degradation after packaging. The main performances are summarized in table 1.

<table>
<thead>
<tr>
<th>Performance</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply</td>
<td>5V +/- 10%</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>5MHz</td>
</tr>
<tr>
<td>Data bus access time</td>
<td>30μs typ</td>
</tr>
<tr>
<td>Package</td>
<td>44pin PLCC</td>
</tr>
<tr>
<td>Power active</td>
<td>25mW typ</td>
</tr>
<tr>
<td>Power stand-by</td>
<td>50μW typ</td>
</tr>
<tr>
<td>13 bit conversion time</td>
<td>8.6μs</td>
</tr>
<tr>
<td>9 bit conversion time</td>
<td>4.0μs</td>
</tr>
<tr>
<td>Watchdog (2 limits)</td>
<td>1.6μs</td>
</tr>
<tr>
<td>Linearity error before cal.</td>
<td>+/-4LSB typ</td>
</tr>
<tr>
<td>Linearity error after cal.</td>
<td>+/-4LSB max</td>
</tr>
<tr>
<td>Full scale error before cal.</td>
<td>+/-4LSB typ</td>
</tr>
<tr>
<td>Offset error after cal.</td>
<td>+/-4LSB max</td>
</tr>
</tbody>
</table>

Table 1: Main performances
Conclusion

An integrated data-acquisition system has been presented. It has been specially designed for an easy implementation inside high speed microprocessor systems without yielding any of its performances and without slowing down the overall system.

References
