Nano-Electronics will be Asynchronous

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All nanoscale technologies that are being proposed to replace CMOS, including nano-CMOS itself, will be unreliable: great parameter variations and high defect rates should be anticipated. Timing will be difficult to control and predict. Noise will be important. Soft errors will appear even at ground level. In many cases, like molecular nano-electronics, nanowires will be short, precluding the implementation of a global clocking network directly in nano. Consequently, asynchronous (clockless) logic seems an ideal, and probably unavoidable choice, for the design of digital circuits in nanotechnology. In this talk, I will report on a preliminary investigation in implementing asynchronous QDI logic in molecular nano-electronics, taking into account the restricted geometry, the lack of control on transistor strengths, the high timing variations. I will show how the main building blocks of QDI logic can be successfully implemented in a somewhat idealized molecular nanotechnology: I will illustrate the approach with the layout of an adder stage. Simulations will be used to demonstrate the remarkable robustness of those circuits in the presence of parameter variations and noise. Most results apply to nano-CMOS as well.