Board and System Level Memory Cluster Test
Problems and Proposed Solutions

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Memory devices have been becoming more complex with every generation and this trend will continue. Different kinds of memories present different challenges for board level test applications. This IP session will discuss several of those challenges and will introduce a new test technology proposed as IEEE P1581, offering an elegant solution to many – if not all – problems related to the test of the board and system level connectivity at memory device pins.

Presentations

State of the Art in Memory Cluster Testing at Board and System Level
Heiko Ehrenberg, GOEPEL Electronics and Roger Sowada, Honeywell

Challenges Related to Memory Cluster Tests
Roger Sowada, Honeywell