Fault Tolerant Nanoscale Architectures — The Challenges and Emerging Solutions

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Design technologies for integrated systems beyond the CMOS era will present new challenges to address the ever important reliability issues. For nanometer-scale processes, it is difficult to guarantee correct fabrication with an acceptable yield without employing design techniques that take into account the intrinsic existence of manufacturing defects. In order to improve the yield and reliability of systems, manufactured with nanoscale devices and wires, their interconnect infrastructures must be designed such that fabrication and life-time faults can be tolerated.

The defect prone manufacturing methods for nano structures are attracting research attention in both academia and industry. The bottom-up chemical synthesis techniques can build nanometer-scale wires and devices. But the main challenge is to create a reliable system out of these inherently unreliable components. Reliability of nano-scale interconnects is a big issue due to inherent limitation of the manufacturing process. It is critical for the R&D community to quickly come up with efficient cost-effective solutions for building and manufacturing nanoscale systems that not only yield acceptably post-fabrication but are in addition well able to provide reliable service while deployed in the field. This session proposes to highlight the real new challenges, and highlight some emerging solutions to this problem. The anticipated speakers would represent views from both academia and industry. Our preferred format would be a session comprised of a series of presentations in which the speakers would present complementary perspectives on the problems and their solution approaches.

Presenters

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