Session 11C — IP Session: Impact of Variations on Design and Test

Organizer: James Tschanz, Intel Corporation

As device dimensions continue to scale with every process generation, the impact of variations of all types is becoming more pronounced. Static process variations — due in part to the widening gap between the process dimensions and the wavelength of light used in lithography — are worsening, while dynamic reliability degradation and aging is becoming a severe problem. At the same time, environmental variations in supply voltage, temperature, and noise are also increasing in importance as circuits are packed more tightly on a die. These variations, which ultimately impact the frequency and power consumption of the fabricated design, have traditionally been handled through a combination of circuit design as well as margining of the frequency and voltage for the final product. However, as variations increase and power constraints are tightened, this margining approach is non-optimal. This session will examine how industry designs have accounted for variations — from the design phase to the operation of the system itself, and considers the challenges that lie ahead in testing these variation-aware designs.

Presentations:

Process Variation Impacts on ASIC Timing and Leakage
Paul Zuchowski, IBM

Process Variation in Nanometer ASICs and SoCs: Problems, Implications, and Solutions
Rich Laubhan, LSI Logic

Testing a Moving Target: Validation of an Adaptive Microprocessor
Eric Fetzer, Intel