Ability to ramp a chip on time is very critical to the success of a product due to short product lifetimes. However, in the nanometer era, shrinking geometries, sub-wavelength lithography, use of new materials (Cu and low-k) and the new processes (CMP) are making this task extremely difficult. Moreover the distribution of the yield loss mechanisms is changing as well. Yield loss is being dominated by the systematic design-process interactions rather than random defects. This renders the learnings from the previous technology nodes inapplicable to the new technology nodes. While the design tools are trying to invent new techniques (e.g. OPC) and new rules (e.g. DFM) to minimize the yield loss, their combined efforts are not sufficient to prevent the significant yield loss. Moreover, the design complexities make the application of some of these techniques impractical. Thus it becomes imperative to use real silicon to understand the yield loss mechanisms. Moreover, to understand the systematic design-process interactions, it is necessary to obtain the fail information inside the chip. Scan diagnosis from the test data can be used to gather fail information inside the chip. However, unlike in debug mode, it needs to be done in a production environment and over a significant volume leading to a “Volume Diagnosis” environment. This requirement of performing diagnosis in a production environment over significant volume requires that a diagnosis flow/system be efficient with minimal impact on the production. This panel will discuss the challenges and requirements of enabling such a system to meet the requirements of yield learning and volume production.

Panelists:

Nagesh Tamarapalli, Mentor Graphics
Tom Jackson, Cadence Design Systems
Tom Williams, Synopsys Inc
Ismed Hartanto, Avago Technologies
Davide Apello, ST Microelectronics