The race to get to the market with high volume quality products demands shorter design to manufacturing cycle forcing increased usage of IPs from multiple sources in SoC designs. The shorter time-to-volume (TTV) requires faster silicon bringup with high degree of diagnosability. In an SoC populated with IPs, this is possible only if the IPs can be isolated during test and debug activities. The IEEE standards committee has now developed a new standard IEEE 1500 which defines an isolation mechanism for IPs (cores) whereby cores with 1500 wrapper can be isolated for test and debug on an SoC. This panel from multiple disciplines of electronics industry will debate on the adoption and application of this emerging standard.

Panelists:
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