Special Session 3
Hot Topic Session

Soft Errors and Tolerance for Soft Errors

Organizer: Eric Dupont, iRoC
Moderator: Joe Borel, ST Microelectronics
Panelists: Jim Chung, Compaq
N. Derhacobian, Virage Logic
Jean Gasiot, Univ of Montpellier
Michael Nicolaidis, iRoC
David Towne, Sun Microsystems
R. Velazco, TIMA

Abstract
IC technologies are approaching the ultimate limits of silicon in terms of channel width, power supply and speed. By approaching these limits, circuits are becoming increasingly sensitive to noise. The reduction of VDD voltage and geometry shrinking implies the reduction of node capacitance. This will increase the ICs sensitivity to alpha particles and atmospheric neutrons, creating unacceptable rates of soft-errors. Thus, the "soft errors issue" is definitely becoming a major consideration for any system developer, especially as we move towards low-voltage VDSM devices. Furthermore, defect behavior is becoming more and more complex resulting on increasing number of timing faults that can escape detection by fabrication testing. Thus, systems houses, IDM or IP provider have to get prepared to IC sensitivity to transient errors, even for commodity applications at sea level: the ability to integrate millions of logic gates and megabytes of memory warrants the scrutiny.

After a reminder on the state of art in Soft Errors issue, this session aims at providing the main trends in Soft Errors sensitivity concerning commodity ICs (mainly processors), as well as existing and future solutions to deal with that new challenge.