Invited Talk

Challenges in Future Technologies

Kamran Eshraghian
Foundation Professor
Edith Cowan University and The University of Adelaide, South Australia

Abstract:

The rapidly emerging area of Ultra High-Speed processing that underpins the transformation of new concepts into working systems necessitates for evolutionary changes in not only the technology base and the strategy for physical mapping of such systems, but also the all important issue of testability and testing. The systems that are mostly affected, and indeed in the next decade or so would require an ever increasing processing power, include real-time signal processors and image processors, computer vision, telecommunications, biomedical systems and personal interactive communicators having processing capability that far exceeds that of the present day super computers. Advances in conventional CMOS over the years have been based on device scaling. As submicron dimensions are approached, further scaling of CMOS becomes increasingly complex and fundamental limits will soon emerge. Paralleling the developments in submicron MOS technology, some evolving technological changes are also beginning to take place in other areas such BiCMOS, Porous Silicon, SiGe Heterostructures, III-V and II-VI compounds, and more recently, Polymer Electronics and Photonics.

For example, advantages of the Bipolar transistor are being utilized as CMOS speed enhancer for it’s greater current drive per unit area, low delay sensitivity to load variation (making excellent line drivers and decoders for memory elements and fast on-chip cache), better device matching, low sensitivity to process variation, and linear performance. Alternatively, Gallium Arsenide is a different material to silicon. For the same power consumption, the first generation GaAs is about half an order of magnitude faster than emitter-coupled logic (ECL), the fastest of the silicon family. Other advantages of Gallium Arsenide over silicon include its higher temperature tolerance, radiation hardness, and optoelectronic properties. The last point permits efficient integration of electronic and optical devices, on the GaAs IC, and is somewhat critical for Ultra High-Speed systems of the future. This creates new opportunities toward on-chip integrated optical communications. Optical interconnect can either take the form of optical fibers or thin film paths (e.g., aluminum oxide) integrated over an area, whole or system. This can be utilized to supply a high-speed global clock to a VLSI circuit without the usual routing complexity.

The possibility that emerges, is for GaAs to be utilized for front-end processor sections of high-speed single stream processors for digital data, usually generated by way of very wideband image sensors, detectors, or the like. This fast data stream can subsequently be subdivided into lower rate parallel streams suitable for processing in silicon CMOS/BiCMOS subsystems at lower frequencies. The necessity for high clock rates in the “front end” processors is compounded since it is very likely that 10-20 microcycles of the processor may be required to pre-process each incoming data sample. This means an input data rate of 10^8 bytes per second might demand a system clock rate of 2 GHz. By mixing GaAs and Silicon CMOS/BiCMOS technologies, it becomes possible to exploit high-system clock rates in a number of systems including high bandwidth signal and image processors, memories, microprocessors, and telecommunication networks.

In the early 1900’s, Abdul Baha called this century the “Century of Light” in anticipation of the revolution that would take place in the mind of mankind. Since the invention of the transistor in 1947, and the development of the very first integrated circuit at the beginning of 1960, there have been four generations of ICs. Now, we are witnessing the emergence of the fifth generation of ICs in the form of MCM, that will be characterized by complexities in excess of 10-20 million devices where integration of Photonics (control of photons) with that of Electronics (control of electrons), will provide the arena for creativity in this new design paradigm. William Bragg once said, “The important thing in science is not so much to obtain new facts as to discover new ways of thinking about them.”
Biography:

Kamran Eshraghian is the Foundation Professor of Computer Communication and Electronic Engineering at Edith Cowan University in Western Australia, and Adjunct Professor of Electrical and Electronic Engineering at The University of Adelaide, South Australia. He obtained his Ph.D., M.Eng.Sc., and B. Tech. degrees from the University of Adelaide, South Australia. He is a distinguished world expert in the field of VLSI systems and circuits. His achievements include pioneering research in CMOS VLSI technology encapsulated in the standard text *Principles of CMOS VLSI Design: A Systems Perspective*, used in over 500 universities throughout the world. He is also the editor of the *Silicon Systems Engineering* series published by Prentice Hall.

In 1977, he joined the Department of Electrical and Electronic Engineering at the University of Adelaide after spending ten years with Philips Research, both in Europe and Australia. He has lectured widely and presented numerous workshops and courses in the United States, the United Kingdom, Europe, Singapore, New Zealand, and Australia. Professor Eshraghian has held a number of visiting academic posts including visiting Professor of Computer Science at Duke University, Professor of Microelectronics & Computer Systems at EPFL, Lausanne, Switzerland, and Professor of Microelectronics at CMA, Spain. He co-founded two successful Australian High Technology companies, providing intimate links between university research and industry. His most recent accomplishment is his contribution towards the design of Australia's first GaAs VLSI systolic processor, based on a new methodology formulated by Professor Eshraghian for GaAs, referred to as the “Ring Notation.” He is a fellow of The Institution of Engineers, Australia.