Foreword

Welcome to the 1995 VLSI Test Symposium, the thirteenth in a series that explores developing trends and the “state-of-the-art” in the area of electronic circuit and system testing. The competitive drive to increase profitability by reducing time to market is made more difficult each year by the continual and rapid increase in complexity of VLSI systems. Through the use of design automation, system design cycles have been shrinking quickly and this, coupled with increasing levels of I.C. integration, has led to the situation where test development now consumes a major portion of the development cycle of VLSI products. The competing demands to offer better products faster, necessitates the use of new and automated test approaches. The theme of this year’s symposium is “Test Automation: Reducing Time to Market,” and the focus will be on novel test automation approaches and methodologies that allow complex electronic products to be brought to market faster. To facilitate test automation, Design for Testability (DFT) is increasingly being adopted. However, rather than being seen as a way of shortening total system development time, DFT has been perceived by some designers as an additional burden that can result in an increase in design effort. This apparent conflict between design and test will be addressed by our keynote speaker, Fred Buelow, Vice President of Technology at Hal Computer Systems, who will discuss the issues involved in reducing Time To Market, particularly in relation to perceived conflicts with DFT.

The two-and-a-half day technical program continues with sessions on hot topics such as BIST, Iddq testing, test synthesis, and delay-fault testing. Panel sessions have proven to be popular with VTS participants, and six are featured again this year. Expert practitioners will discuss current issues such as test standards (in sessions on both the 1149.5 and QTAG Iddq monitor activities), how deep sub-micron process technology will influence test requirements, and high-level test synthesis using realistic fault models. Also included this year are two tutorials on high-level DFT and on-line testing — topics currently of very high interest to many in our audience.

There were a record number of high-quality submissions this year, and so paper selection was a difficult task. Out of a total of 150 papers submitted, only 70 could be included in the program. Papers were selected on the basis of a rigorous review procedure, with over 250 reviewers participating in the review process. The final selection was made by the program committee, which met simultaneously in three locations in the US and Canada, linked via a video-conference line. The video-conferencing facilities were generously provided again this year, as they were for VTS’94, by AT&T and BNR, and we thank them for their continued support.

VTS is truly an international event, with submissions this year from 25 countries. This year, for the first time, the majority of submissions were from countries outside of the US, with the number increasing over the previous year from 42 percent to 57 percent of total submissions. The significant international participation truly reflects the maturity of this symposium as a major forum for the informal exchange of new ideas in VLSI testing.

The VLSI Test Symposium is the result of the volunteer work of over 250 dedicated test professionals. In particular, the symposium and program committee members have made significant contributions toward the success of this symposium and we would like to thank them wholeheartedly for their efforts. That the program committee has been able to put together an excellent program is a direct result of the high quality of the submissions. Thus, we would also like to thank the program participants for submitting their work and agreeing to present it at the symposium. Finally, we would like to thank the IEEE Computer Society, its Test Technology Technical Committee, and the Philadelphia Section of the IEEE for their continued sponsorship and support.

The goal of the VTS committees is to improve the symposium continuously to meet your changing needs and so, please take the opportunity during the symposium to let us know how we can do this better in the future. We welcome your comments and suggestions.

VTS is your symposium and we encourage your active participation. We hope that you will find the 1995 VLSI Test Symposium lively, interesting, thought-provoking, useful, and above all, fun.

Welcome to VTS’95!

Prab Varma 
General Chair

Yervant Zorian 
Program Chair