Special Session:
The Future of NoCs: New Technologies and Architectures

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Motivation for Special Session:

Continuing progress and integration levels in silicon technologies make possible complete end-user systems consisting of extremely high number of cores on a single chip targeting either embedded or high-performance computing. However, without new paradigms of energy- and thermally-efficient designs, producing information and communication systems capable of meeting the computing, storage and communication demands of the emerging applications will be unlikely. In addition, in order to sustain the predicted growth of number of embedded cores in a single die, it is extremely important to have a scalable, low power and high bandwidth on-chip communication infrastructure. Towards this end, Network-on-Chip architecture incorporating various emerging interconnect paradigms is an enabler for designing low power, high bandwidth multicore chips. Innovative interconnect paradigms based on optical technologies, RF/wireless methods, carbon nanotubes, or 3D integration are promising alternatives that may indeed overcome the challenges encountered. These open up new opportunities for detailed investigations regarding the possibility of building NoCs with the emerging interconnect infrastructures.

The emerging field of NoC with Photonic, Wireless and 3D interconnects is actively being pursued by a number of researchers worldwide, from a variety of different perspectives, ranging from very high levels of abstraction (e.g., system architecture) to very low levels (physical layer and transceiver design). Successful solutions will likely adopt and encompass elements from all or at least several levels of abstraction and rely on interdisciplinary concepts from multi-core architectures, integrated circuits, silicon photonics, 3D IC, digital communications, complex networks, and optimization techniques. Hence, we believe that our special session can provide a timely and insightful journey into various challenges and emerging solutions regarding the design of future NoC architectures. By scope and contents, this special session represents an engaging proposition to attendees belonging to both academia and industry.

The general objective of this special session is to create a focused forum on the characteristics of NoCs build with novel emerging interconnect paradigms. The session will aim at successfully achieving at least two goals well within the scope of the VLSI design conference. The first goal will be to expose the attendees to the limitations of traditional planar NoCs, and more importantly to some of the more prominent emerging solutions, and of course present a critical view in regards to advantages, limitations, specific challenges, etc. of these methods. The second important goal of the session will be to provide the NoC experts with a focused forum allowing them, along with the general audience, to contrast the trade-offs of the different solutions from various perspectives.

Organizers’ Biographies

Partha Pratim Pande is a Professor and holder of the Boeing Centennial Chair in computer engineering at the school of Electrical Engineering and Computer Science, Washington State University, Pullman, USA. He received his M.S degree in computer science from the National University of Singapore and the Ph.D. degree in electrical and computer engineering from the University of British Columbia, Vancouver, BC, Canada. His current research interests are novel interconnect architectures for multicore chips, on-chip wireless communication networks, and hardware accelerators for biocomputing. Dr. Pande currently serves as the Editor-in-Chief (EIC) of IEEE Transactions on Multi-Scale Computing Systems (TMSCS) and Associate Editor-in-Chief (A-EIC) of IEEE Design and Test (D&T). He is on the editorial boards of IEEE Transactions on VLSI (TVLSI), ACM Journal of Emerging
Technologies in Computing Systems (JETC) and Sustainable Computing: Informatics and Systems (SUSCOM). He is the technical program committee chair of IEEE/ACM Network-on-Chip Symposium 2015. He also serves in the program committee of many reputed international conferences. He has won the NSF CAREER award in 2009. He is the winner of the Anjan Bose outstanding researcher award from the college of engineering, Washington State University in 2013.

**Sudeep Pasricha** received the B.E. degree in electronics and communication engineering from Delhi Institute of Technology, Delhi, India, in 2000, and his M.S. and Ph.D. degrees in computer science from the University of California, Irvine in 2005 and 2008. He joined Colorado State University (CSU) in 2008. He is currently an Associate Professor in the Department of Electrical and Computer Engineering and the Department of Computer Science at CSU, where he is also the Chair of Computer Engineering and the Director of the Multicore Embedded Computing Systems (MECS) Lab. He also holds an affiliate faculty member position at the Center for Embedded Computer Systems at the University of California, Irvine. He is the recipient of the 2015 IEEE TCSC Award for Excellence for a mid-career researcher, the 2014 George T. Abell Outstanding mid-career faculty award, and the 2013 AFOSR Young Investigator Award. Prof. Pasricha is currently the Editor-in-Chief of the ACM SIGDA E-news, Associate Editor of ACM Transactions on Embedded Computing Systems (TECS), Associate Editor of IEEE Transactions on Multi-Scale Computing Systems (TMSCS), and Advisory Board member of ACM SIGDA. He is currently or has been an Organizing Committee Member of several IEEE/ACM conferences such as DAC, ESWEEK, GLSVLSI, VLSID, NOCS, RTCSA, AICCSA, MWCAS, ICECS and ICCAD CADathalon, as well as Technical Program Committee member of these and several other IEEE/ACM conferences. He is a Senior Member of the IEEE and ACM.

Prof. Pasricha’s research interests are broadly in the areas of embedded systems, mobile computing, and high performance computing, with an emphasis on energy-efficient, reliable, and secure system design. More specific topics of interest include: on-chip network and memory architecture (cache, DRAM) design, emerging technologies such as silicon nanophotonics and non-volatile memories, multi-objective optimization, system-level CAD, real-time embedded systems, and resource scheduling for parallel computing platforms (cloud datacenters, supercomputers). He also works on applications of technology to occupational therapy, automotive systems, robotics, mobile sensing, and workflow automation. He has written a book, contributed several book chapters, and published over 100 research articles in peer-reviewed conferences and journals. His research has been recognized with Best Paper Awards at the ACM GLSVLSI 2015, IEEE AICCSA 2011, IEEE ISQED 2010 and ACM/IEEE ASPDAC 2006 conferences.

**Hiroki Matsutani** is an Assistant Professor at the Department of Information and Computer Science, Keio University, Yokohama, Japan. He received his Ph.D. degree in engineering from Keio University in 2008. His current research interests are on-chip interconnection networks, wireless 3D chip stacking, datacenter networks, and hardware accelerators for databases, distributed data stores, big data analysis, and machine learning. His papers on these topics have been accepted for ISCA, HPCA, NOCS, DATE, IEEE TC, IEEE TPDS, IEEE TCAD, IEEE TVLSI, and IEEE Micro. He currently serves in the Program Committee member of reputed international conferences including NOCS, DATE, ISLPED, and CODES+ISSS. He has served in the Organizing Committee member of NOCS 2016, MPSoC 2016, ISLPED 2015, and MCSocC 2013. He received the Best Paper Awards from HEART 2015 for machine learning accelerators, ASP-DAC 2013 for wireless 3D NoCs, and ICNC 2011 for HPC interconnects. He was awarded a Research Fellowship of the Japan Society for the Promotion of Science for Young Scientists SPD from 2009 to 2011.

**Contributed Presentations in the Special Session**

**Millimeter (mm)-Wave Wireless NoC as Interconnection Backbone for Multicore Chips: Promises and Challenges**

Partha Pratim Pande

**Abstract:** The latency, power consumption, and interconnect routing problems of NoCs can be simultaneously addressed by replacing multi-hop wired paths with high-bandwidth single-hop long-range wireless links. In this talk, we will present design of the millimeter (mm)-wave wireless NoC architectures. We will present detailed
performance evaluation and necessary design trade-offs for the small-world wireless NoCs with respect to their conventional wireline counterparts. We will also discuss different media access control (MAC) mechanisms and routing protocols used for Wireless NoCs so far. To sustain the predicted performance, a deadlock-free routing algorithm must be designed. The routing protocol also needs to be simple without incurring excessive power, area and latency overheads. We will finish this presentation by discussing the thermal and power management policies suitable for Wireless NoCs.

**Illuminating the Future of Multicore Computing with Silicon Nanophotonic NoCs**  
*Sudeep Pasricha*

**Abstract:** Silicon nanophotonics represents one of the more promising solutions to overcome the challenge of worsening on-chip communication performance in emerging multicore platforms. By transferring data using light signaling between cores and memory, orders of magnitude improvement in bandwidth, latency, and energy are possible. Silicon nanophotonics also promises to pair well with existing board-to-board and chip-to-chip photonics offerings that are rapidly being adopted today. Not surprisingly, many semiconductor companies such as Intel and IBM have begun investing heavily into silicon nanophotonics. This talk will present some of the recent innovations in architectures, protocols, and models to enhance performance, energy-efficiency, and reliability for silicon nanophotonics. The first part of this talk will focus on 2D and 3D NoC architectures that dynamically partitioning application traffic between electrical and photonic links, and adapt various NoC design parameters over time to achieve significant performance and energy improvements for on-chip communication. The second part of the talk will focus on protocols for photonic on-chip communication. In particular, we will discuss a smart arbitration protocol to improve utilization of on-chip photonic links and enhance overall communication efficiency. Next we will discuss models for crosstalk characterization in photonic waveguides and microring resonators. We will present techniques to improve transmission reliability in the presence of crosstalk noise. Lastly, we will explore extensions of silicon nanophotonics to beyond the chip, to improve communication performance with photonic links between multicore processors and high-bandwidth main-memory modules.

**Inductive-Coupling 3D Wireless NoC Designs**  
*Hiroki Matsutani*

**Abstract:** 3D integration is a promising solution to integrate more processors, memories, and accelerators without increasing the wire delay. Various 3D integration technologies have been developed to connect stacked wafers or dies: microbumps, through-silicon vias (TSVs), and wireless technologies, such as capacitive-coupling and inductive-coupling. In this talk, we will focus on wireless 3D NoCs that use the inductive-coupling though-chip interfaces (TCIs) to connect stacked chips by using square coils, because it has a scalability to stack more than two chips and a flexibility of the contact-less approach. The inductive-coupling TCI is a low-cost 3D integration solution, as data transceivers are implemented with metal layers of common CMOS process. We have been developing some prototypes 3D systems using inductive-coupling TCIs, where an arbitrary number of processor chips, accelerator chips, and memory chips can be selected and stacked. We are also developing a key-value store memory chip for the 3D systems so that processors can store computational or intermediate results in a key-value form. In this talk, we will introduce two topics: 1) design and implementation of the wireless 3D systems in which an arbitrary number of processor chips, accelerator chips, and key-value memory chips are interconnected with a wireless 3D NoC and results from its prototyping fabricated with a 65nm process; 2) novel interconnection techniques for the wireless 3D NoCs that cover wireless broadcast bus design, routing and flow control schemes, and some optimization methods for improving the energy and performance.