Tutorial: An introduction to VHDL 2008

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Abstract

Design and verification of digital circuits involves describing behavioral functionality using HDL (Hardware Description Language). Given the fact that modern day designs have grown significantly in terms of complexity and size, there is a very obvious requirement to have powerful languages which can offer constructs and methodologies which not only cater to these requirements, but can also facilitate development of highly reusable and error free code leading to reduced development cycles and more efficiency.

VHDL (VHSIC Hardware Description Language) was first developed on requirements of U.S Department of Defense which was later adopted as an IEEE standard first in 1987. The primary goal of the language was to provide a suitable environment for designers to design development and verification side by side. Till date VHDL is perceived as a very powerful HDL which offers wide range of constructs specifically targeted to aid in development of highly reusable code. Since it is a strongly typed language it leaves minimal scope for errors in the designs.

In order to keep in pace with design requirements VHDL has gone several revisions. VHDL 2008 was the most significant revision done to VHDL with last major revision being way back in 1993. This tutorial is designed to explain the new features of VHDL 2008 and its value to both the RTL designer and verification engineers. This tutorial program will discuss all the important enhancements to the language with proper examples along with an emphasis on the possibilities to reduce the VHDL code size with the recent language changes. This tutorial will also explain the usage with older version of VHDL and new VHDL side by side for better understanding. It will discuss major enhancements done in VHDL 2008 standard and some features which are introduced in VHDL 2008 to bridge the gap with respect to design methodologies offered by other standard hardware description languages.

Speakers Biographies
**Kausik Datta** has over 20 years of experience in engineering and management at the EDA industry. Currently he is working as Senior Manager at Mentor Graphics (India) Pvt. Ltd., Kolkata and leading the “Front-end Analyzer Group”. Prior to working with Mentor Kausik had worked with Interra Systems, Delsoft and Siemens on software development in EDA and Telecom domain. Kausik received his Bachelor of Engineering degree in Electrical Engineering from Jadavpur University, and his M. Tech. in Computer Science from the Indian Statistical Institute, Kolkata.

**Goutam Kumar Bhaumik** has over 20 years of working experience with EDA, CAD and Semiconductor industries. Currently he is working as Staff Engineer at Mentor Graphics (India) Pvt. Ltd, Kolkata Development Center and playing key roles in the “Front-end Analyzer Group”. Prior to working with Mentor, Goutam worked with Interra Systems, Delsoft and Semiconductor Complex Limited where he worked on software development in EDA and CAD domains, Library Characterizations, IC Process Design, Device Simulations, etc. Goutam completed Master in Physics from Jadavpur University and M. Tech in Material Science (Semiconductor) from Indian Institute of Technology, Kharagpur.

**Rohit Goel** has over 11 years of experience in engineering in EDA industry. Currently he is working as Staff Engineer & Manager at Mentor Graphics (India) Pvt. Ltd., NOIDA in the “Front-end Compiler Group”. Rohit received his Bachelor of Engineering degree in Electrical Engineering from Indian Institute of Technology Varanasi (Formerly Institute of technology, Banaras Hindu University)