Embedded Tutorial ET2

Volume Diagnosis for Yield Improvement

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Abstract

Process variations in sub-nanometer technologies cause systematic defects in manufactured VLSI devices. Such defects may be process dependent as well as design dependent. This requires identification of root causes for systematic defects to aid device yield ramp up. Volume diagnosis or diagnosing a large volume of manufactured devices is necessary to identify systematic defects. Volume diagnosis requires highly efficient and effective software tools since physical failure analysis of a very large number of failing devices is not practical. Typically volume diagnosis uses two procedures. First, responses from failing devices are analyzed using defect diagnosis tools. Next the results of diagnoses are analyzed using statistical, data mining and machine learning techniques to effectively determine the underlying defect distribution for yield improvement. In this presentation, we will discuss diagnosis procedures and methods for analyzing diagnosis data in a typical software based volume diagnosis flow. We will also briefly discuss topics for future research in volume diagnosis.

Conventionally, yield improvement is based on physical failure analysis of several failing devices to identify root causes for failing devices. This process is time consuming and expensive due to physical failure analysis (PFA) times. Traditionally, most PFA techniques involved incremental cuts and inspection. With relatively high probability of via open failures in 90nm and smaller technologies, it is a significant effort to open a failing die to view a specific failing via clearly. This process is destructive and thus it is important to have accurate prior knowledge of defect locations before initiating PFA. To have this knowledge, it is necessary to rely on diagnosis software to identify the defect locations. Software-based diagnosis of the failing devices can determine the defect type and location for each failing device based on the design description, scan test patterns, and tester fail data. With layout-aware diagnosis, it can provide further resolution with detailed defect physical information, which significantly improves PFA success rate. Recently, FinFET transistors bring new challenges to PFA. To inspect transistor fins, it requires the use of transmission electron microscopy (TEM), which in turn requires a one-shot prep and inspect. To achieve this, diagnosis results need to be able to point to a single or very few transistors. This has triggered the development of transistor-level (or cell-aware) diagnosis, and defect diagnosis is now a “must have” rather than a “nice to have” in the PFA process.

However, higher PFA success rate, does not guarantee ability to identify common root cause of defects, to improve yield, through a handful of PFA analyses. To have enough samples with common root causes, it is important to use statistical methods on a large volume of diagnosis data to identify which failing dies should be subjected to PFA so as to increase the probability to identify common root cause(s) for failing devices. In yield analysis, knowing what common features exist at different defect locations is also crucial. Recently, statistical methods, such as Root Cause
Deconvolution (RCD) are used to remove the noise in the diagnosis results. Multiple layout-aware diagnosis reports are analyzed together with machine learning capability in RCD to identify the underlying common root causes and significantly increase the success rate of identifying root cause(s) of defects. For instance, layout-aware diagnosis may point to a net segment that spans multiple layers as the possible location of an open defect. RCD narrows this result down to a common specific VIA type in this net segment. This dramatically reduces the PFA time by increasing the PFA success rate. It also enables “virtual PFA”, the ability to determine accurate defect distributions for a population of failing devices before any PFA is performed. This technology makes volume diagnosis effective to speed up the yield improvement process.

As shown in the diagram for volume diagnosis flow, given below, RCD requires layout-aware diagnosis result from a number of failing die, for instance all failing devices on one wafer. The technology leverages design statistics such as critical area per net segment per layer and count of tested cells per cell type. It uses known machine learning techniques and a probabilistic model that calculates the probability of observing a set of diagnosis results for a given defect distribution. This model is in turn applied to determine the most likely defect distribution for a given set of diagnosis results.

At modern technology nodes, root cause of yield loss is often found to be due to specific design structures. Certain designs may have lower yield than comparable designs using the same manufacturing process. This means that the yield analysis capabilities that were previously only required in foundries are now required at fabless companies also. This has also brought the need for layout pattern analysis; the ability to identify yield-limiting layout structures. Volume diagnosis is a significant component of this capability. In practice, fabless companies use diagnosis results to enable the foundries in identifying yield issues faster. Foundries use diagnosis results to compare fail mechanisms across multiple designs, IPs, and manufacturing processes to improve manufacturing processes.

**Speaker Biographies**

**Wu-Tung Cheng** is a Chief Scientist and Advanced Test Research Director in Mentor Graphics. He is an IEEE fellow since year 2000. He has over 135 publications and 41 patents. In 2006, he received ITC best paper award. In
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Sudhakar M. Reddy is a University of Iowa Foundation Distinguished Professor. He is a life Fellow of IEEE. He received the first Lifetime Achievement Award from VLSI Design Conference and received a Von Humboldt Foundation Prize in 1995. He has published over 600 papers and has guided over 40 Ph.D. students.