Tutorial T3B

Engineering Change Order (ECO) phase Challenges and Methodologies for High Performance Design

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Abstract

Engineering Change Order or ECO phase is always challenging for any family of chip design. High Performance Microprocessors are largest and most complex overall design within Semiconductor Industry as a whole. To add further, there are additional design and methodology challenge related to bleeding edge of process nodes. Hence, current and future microprocessor design requires a set of well planned and innovative methodologies to cater to the ECO requirement when the race to the finishing line begins! This tutorial is organized into following four key sections. Apart from that, there will be a brief preview section and a real scenario-based learning section towards the end.

ECO Readiness Indicator: Before a design can actually enter an ECO phase, quite a few things needs to be assessed. Some of the key indicators are logic and verification stability from front-end team, timing, power, routability, noise and other metrics from backend or circuit team. ECO phase can achieve only limited set of changes and hence design stability needs to be thoroughly evaluated. Also, during mainstream design closure process, ECO preparatory study and optimizations need to be performed. Typically it includes ensuring sufficient ECO resource availability following a good distribution in all part of design. ECO resources include spare latch, Gate-Array cells among others.

ECO Variants: After ensuring ECO readiness indicators are achieved, designers need to know nature of ECO requests that might come in. This can be categorized based on timeline (full stack comprising of device and metal stack usage for ECO or limited metal stack usage type) or based on ECO objective. Typically, there are two basic flavor of ECO objective – Functional or Performance based. Functional ECOS arise because of last moment verification bugs caught or critical enhancement components. Performance based ECOS occur for different changes made to optimize timing across hierarchical boundary, change in timing constraints or other dependent changes. There can be minor but other kind of requests related to power, noise etc.

CAD for ECO: ECO CAD framework typically consists of a ECO extraction engine, ECO stitching and ECO physical synthesis engine. ECO extraction engine uses a SAT solver based functional equivalence checker, logic structural matching algorithm internally. ECO stitcher merges the ECO logic elements to original Netlist but it is not synthesized and placed yet. ECO physical synthesis segment perform actual physical synthesis optimization ECO implementation. This engine opens up a limited logic cone (1- or 2-hop neighborhood) in ECO delta region for timing/power/other convergence criteria. Finally, incremental ECO routing is performed to build the complete
design. ECO Implementation Strategies: After the ECO requirements are analyzed in terms of technical challenge, risks and time in hand, a suitable methodology is adopted to get it done. On a broader level, it is taken through either a ECO tool based methodology or manual ECO methodology. Sometime both approach are tried in parallel to save time. ECO tool based methodology typically supports multiple CAD recipes depending on ECO complexity, amount of change requested for most efficient ECO solution that comes with least change in design. Manual ECO approach on the other hand counts on skill of individual engineer identifying the ECO location and getting functional equivalence or timing targets achieved after the changes made.

**Post ECO Design Closure:** After primary objective of the ECO is met, the entire design needs to be taken through a set of quality checks to make sure it is of tape-out quality. In most cases, there will be secondary optimizations based on additional design violations created while trying to achieve primary ECO needs. These violations are fixed in subsequent design iterations.

**Speaker Biographies**

**Sridhar Rangarajan** received the B. Tech. (Hons.) degree in Computer Science and MSc. (Hons.) in Economics from BITS, Pilani and M.S. in Computer Science and Engineering from Santa Clara University USA. He has around 15 years of EDA experience leading various positions primarily in physical design domain. Currently at IBM, he is leading the development effort of tools and methodologies for next generation microprocessors. Before joining IBM, he was working in Synopsys where he involved in developing the next generation router. He also held various technical positions in Sun, Monterey Design Systems and Cadence, involved in developing physical design tools and solutions. His research interests include CAD VLSI for physical design, routing, DFM, combinatorial optimization, graph algorithms.

**Pinaki Chakrabarti** did his Bachelor of Engineering in Computer Science & Technology from Bengal Engineering College, Howrah, West Bengal in 1997 and completed his Master of Technology in Computer Science & Engineering from Indian Institute of Technology, Kanpur in 2000. Pinaki in his 14+ years of work experience, worked in Wipro Technologies, Mentor Graphics India and Synopsys India. Currently he is working at India Software Lab in IBM India. His interests include computer architecture, low power physical synthesis and clock tree/mesh physical synthesis.

**Sourav Sahais** a Senior Engineer at IBM Processor Division, Bangalore currently engaged on Instruction Fetch Unit design for Z series microprocessor. He received his Masters degree from IIT Roorkee in 2005 and served at Intel and ARM prior joining IBM in 2010 on processor research prototype and memory IP design respectively. Sourav has presented several papers and tutorials in IEEE conferences and also has 1 granted and 4 filed patents. His research area includes physical design, noise-thermal aware design, variability tolerance etc.

**Ayan Datta** is a Research and Development engineer at IBM Bangalore, where he is leading the common library design for IBM’s System Z. He received his Master Degree from Jadavpur University at 2008. Since then Ayan is a part of IBM India Systems and Technology Hardware Development Lab. Ayan has served on the technical program committee of IEEE conferences. He has presented papers in recent years at ISVLSI and VLSI Conferences. His research interests are in Finfets, Engineing change order, reliability and 3D design.

**Adarsh Subramanya** completed his Bachelors in Engineering from M.S.Ramaiah institute of engineering in 2007. He joined IBM in the same year and has worked on physical design over several generations of IBM Power processors. He currently leads the physical design activities of PCIe components of the chip.