Tutorial T3A

Testing Low-Power Integrated Circuits: Challenges, Solutions, and Industry Practices

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Abstract

The push for portable, battery-operated, and “cool-and-green” electronics has elevated power consumption as the defining metric of integrated circuit (IC) design. Testing ICs built for such applications requires judicious consideration of test power implications on various aspects of the design cycle (e.g., packaging and power grid design), test engineering (multi-site ATE power supply limitations and board design), power-aware test planning (DFT and ATPG), and developing the enabling EDA tool infrastructure (SW for estimation, reduction and low-power test generation). Physically-aware low-power test techniques are also becoming important for accuracy and hot-spot minimization, especially for designs at 22nm and below. Furthermore, with power optimization and power management techniques becoming “de-facto” in almost all 45nm and lower chips, systematic testing of these structures and the device in the presence of these structures becomes mandatory. This tutorial is intended to provide an in-depth and up-to-date understanding of low-power IC testing covering (a) dimensions of power-aware testing, (b) methods for test power analysis and signoff, (c) techniques for controlling test power consumption and (d) test of power managed designs. Case-studies illustrating industrial design deployment practices and existing EDA vendor support will be outlined to illustrate capabilities and gaps in the state-of-the-art.

Speaker Biographies

Srivaths Ravi is a Design Manager, and Member of Group Technical Staff with the Processor Group at Texas Instruments, India, where his team is responsible for DFT implementation for some of TI's low-power chips. At TI India, he has also been responsible for furthering test methodology initiatives in power-aware test, scan compression, and ATPG, and test tool deployment across different business units. Prior to TI, Dr. Ravi was a research staff member with NEC Laboratories America, Princeton, where he was mainly responsible for R&D projects in embedded security and low power design. His work at NEC has contributed to the design of a low power security processor MOSES used in NEC’s cellphone chips, as well as to the development of RTL and C-based power estimation capabilities in NEC’s Cyber design framework. His contributions have also been recognized with NEC Laboratories’s Technology Commercialization Award.

Dr. Ravi has nearly hundred publications in the areas of test, low power EDA, and embedded security. He has so far received seven best paper awards and seven granted patents. He serves in the organizing and technical program
committees of various leading conferences. Most notably, he was the Program Co-chair of the 2011 Asian Test Symposium (ATS), Vice Program Co-chair of the 2011 VLSI Test Symposium (VTS), General Chair of the 2011 VLSI Design Conference (VLSID) and an Associate Editor with the *IEEE Transactions on VLSI Systems* (TVLSI). He has also held a visiting research collaborator position with the Department of Electrical Engineering at Princeton University and has most recently been a guest lecturer at the Indian Institute of Science, Bangalore.

Dr. Ravi received the B.Tech degree in Electrical and Electronics engineering and the Siemens Medal from the Indian Institute of Technology, Madras, India, and the M.A. and Ph.D. degrees in Electrical Engineering from Princeton University, Princeton, NJ. He is a Senior Member of IEEE.

**Vivek Chickermane** is a Distinguished Engineer and Director of DFT R&D with the Encounter Test team at Cadence Design Systems. He leads a diverse team of technologists and EDA software engineers that develops EDA tools for scan synthesis, test point insertion, IEEE 1149.1 and 1149.6 boundary scan, IEEE 1500 Core Test, XOR and MISR based Test Compression, Logic BIST, Memory BIST, Power-Aware DFT, and more recently DFT for 3D ICs. Prior to joining Cadence in 2002, Dr. Chickermane was a Senior Engineer at IBM EDA, where he lead the development of DFT Synthesis from its inception to the point where they were a key part of IBM ASICS’ Front-end Design and Sign-off kits and deployed world-wide. He was awarded an IBM Outstanding Technical Achievement Award for his contributions.

Dr. Chickermane has contributed to over 60 refereed publications and 18 issued patents covering many aspects of DFT and ATPG. Most recently he and his team have been very active in the areas of Low Power test and 3D DFT and were the first to productize many key innovations. His team’s inventions in the area of using standard power formats for power-aware DFT won them the Cadence’s Excellence in Innovation Award in 2011. He has served on the working groups for IEEE 1149.6, IEEE 1500 and IEEE P1838 and is currently on the Program Committees for ITC and ATS.

He received the B.Tech degree in Electrical and Electronics engineering from the Indian Institute of Technology, New Delhi, India, and the M.S. and Ph.D. degrees in Electrical & Computer Engineering from the University of Illinois, Urbana-Champaign, IL. He is a Member of IEEE.

**Krishna Chakravadhanula** is a Senior Member of Consulting Staff with the Encounter Test team at Cadence Design Systems. He leads the Low Power Test R&D team and has been responsible for driving the innovation and implementation of low-power test strategies and methodologies within the Encounter Test portfolio. This includes implementing Low-Power ATPG techniques for gated clock designs and tools for test power analysis at different design stages. He was a key member of a Cadence-wide initiative to standardize on a methodology for implementing and testing power managed designs by leveraging the Si2 Common Power Format (CPF). He is also responsible for driving advanced test techniques like low-pin compression, at-speed DFT and hierarchical test strategies based on industry standards.

Dr. Chakravadhanula has many publications at leading conferences and journals in the areas of power-aware test and test compression and received a best paper award at VTS 2001. His innovations have resulted in 5 filed patents (2 issued) in the area of power-aware test, and 3 filed patents (1 issued) in related areas. He has also co-authored a book chapter in “Power-Aware Testing and Test Strategies for Low Power Devices”. He is on the working group for IEEE P1687 and serves on the Technical Program Committees of Asian Test Symposium (ATS) and North Atlantic Test Workshop (NATW). He is currently the Program Vice-Chair of NATW 2013.

Dr. Chakravadhanula received the B.E. in Computer Science and Engineering from Jadavpur University, Kolkata, India, and M.S and Ph.D. degrees in Electrical and Computer Engineering from University of Texas at Austin. He was awarded the IBM Ph.D. Fellowship from 2002-2004 and did internships at Synopsys, Agere and IBM. He is a Member of IEEE.