Tutorial T3

Design of Deep Sub-Micron CMOS Circuits and Design Methodologies for High Performance Microprocessor

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Abstract

This tutorial discusses design challenges of high performance CMOS circuits in the deep submicron technologies and the design methodologies required to design them in order to produce robust designs with desired power performance trade-off. This proposal will have following major components:

Opening session: This section is aimed at connecting the audience with key points proposed in tutorial and setting the expectation at right level.

Introduction to technology and scaling challenges, advancement in technology and physical design closure methodologies, power reduction, lithography and reliability related challenges will be briefly introduced in the context of high performance microprocessor design.

Section-1: Challenges in Technology and Device Scaling: To continue scaling of the CMOS devices deep into 22nm technologies and beyond, fully depleted SOI, strained-Si on SiGe, FinFETs with double gate and even further, three-dimensional circuits will be utilized to push the frontiers of high-performance circuits. Unique design aspects and issues resulting from this scaling such as gate-to-body tunneling, self-heating, bias temperature instability and reliability issues, and process variations will be covered in details. As scaling approaches various physical limits, new design issues such as $V_t$ modulation due to leakage, low-voltage impact ionization, and higher $V_{t,lin}$ to maintain adequate $V_{t,sat}$ continue to surface. In this part of tutorial, these emerging trends and design issues related to aggressive device scaling will be discussed.

In this section we will also talk about reliability and yield improvement which are problems plaguing advanced technologies like 32nm and beyond. Reliability issues like BTI degradation, electromigration and how these are screened will be discussed.

Section-2: Design System for developing Very High Performance Microprocessors: With device dimensions approaching their physical limits, design methodologies are playing increasing significant role in achieving desired power and performance. In deep sub-micron designs, chip performance is increasingly limited by the interconnect delay. Transistor delays decrease with technology scaling, while the narrower metal lines and space increase the relative delay associated with the interconnects. With each technology generation, the capacity of a same-sized die...
doubles, and the complexity and gate count of the design grows. The dominant interconnect delays require accurate net length and delay prediction during timing optimization to improve circuit performance. Not only does the design of circuits in 22nm technologies require a high-performance synthesis system but it also necessitates seamless integration of placement and synthesis design environments. In addition, with the coupling-capacitance issues generating increasing difficulties for design closure, more accurate wire routes must be known while optimizing the design in order to fix these problems earlier in the design cycle. This requires close integration of interconnect routing environment with placement and synthesis environments. In this part of tutorial, details of a high-performance synthesis system including dataflow synthesis and planning and a design flow will be presented in which placement, synthesis, and routing environments closely and seamlessly interact with each other to handle flat designs for the highest performance microprocessor design in computer industry, IBM z196, with its record setting performance with frequencies over 5 GHz.

Section-3: Power Optimization Techniques in High Speed Microprocessor: It is well known that with CMOS technologies in 22nm, power is one of the most crucial design components which must be efficiently controlled in order to utilize the performance advantage from these technologies. Various techniques to analyze and control all components of power placing particular emphasis on sub-threshold and gate leakage power will be focus of this section. In addition, this part of tutorial will discuss low voltage circuit design under high intrinsic leakage, leakage monitoring and control techniques, effective transistor stacking, multi-threshold CMOS, dynamic threshold CMOS, well biasing techniques, and design of low leakage data-paths and caches and other methodology improvements related to power optimization.

Section-4: Challenges in Lithography, DFM and Variability: Nanometer design technologies must work robustly under tight operating margins, and are under increasing challenges from lithography and Fabrication. Design closure is therefore highly susceptible to any process and environmental variability. This part of the tutorial will consider several factors related to design for manufacturability, lithography and variability issues in 22nm and state-of-the-art approach to address these problems. Specifically, we will discuss how multiple patterning technologies interact with design in context of layouts and design rules.

Case Study: A brief case study will be covered on the design and implementation of IBM z196 – a high performance microprocessor running at a record 5.2GHz in 45nm technology.

Wrap Up: Closure of the tutorial, a peek at the future of technology, design challenges and what lies ahead of us.

Speaker Biographies

Ruchir Puri is an IBM Fellow at Thomas J Watson Research Center, Yorktown Heights, NY where his efforts have focused on high performance processor and ASIC design and methodology solutions for all of IBM's enterprise server and system chip designs. Most recently, he lead the design methodology of IBM's latest Power7 microprocessor and is currently leading design methodology research efforts on future processors as well. Ruchir has received numerous IBM awards including IBM's highest technical honor IBM Fellow (awarded for his transformational role in microprocessor design methodology). In addition, he has received “Best of IBM” awards in 2011, and 2012 and an IBM Corporate Award from IBM's CEO, and several IBM Outstanding Technical Achievement awards. Dr. Puri is a member of IBM Academy of Technology, an IBM Master Inventor, an ACM Distinguished Speaker, an IEEE Distinguished Lecturer, and a Fellow of the IEEE. Ruchir is a frequent invited speaker and panelist at many leading Design Automation and VLSI design conferences and has served on numerous technical program committees and IEEE journal editorial boards. He is recipient of SRC outstanding mentor award and has been an adjunct professor at Dept. of Electrical Engineering, Columbia University, NY and was also honored with John Von-Neumann Chair at Institute of Discrete Mathematics at Bonn University, Germany.
Charudhattan Nagarajan is a senior engineer at IBM leading the work in Physical design and timing closure in IBM's mainframe processors. He has a Masters in MicroElectronics and Masters in Physics from BITS, Pilani. He has about 16 years of industry experience mostly doing physical design for ASICs and microprocessors. His main interests are methodology development and physical design for high performance microprocessors and ASICs. Charu has 2 patents and 5 publications in the field of physical design. He also serves as technical committee member for reviewing invention disclosures at IBM.

Sourav Saha is a senior engineer at IBM processor development team at Bangalore currently involved in processor core design of Z series microprocessors. He has Masters in Solid State Electronics from IIT Roorkee. He has 7 years of industry experience in the area of processor and memory IP design. Prior joining IBM, he worked in Corporate Technology Group (Circuit Research Lab) at Intel Bangalore developing Terascale processor prototype and Memory IP group at ARM Bangalore and Austin where he was involved at different flavor of memory compiler development. His research interests include early prediction and mitigation of physical design issues, thermal optimization in physical design, low power design, variability and reliability modeling and characterization. Sourav has 1 granted US patent and multiple internal and external publications.

Rahul Rao is a senior engineer at IBM Bangalore, where he is a technical lead of IBM’s P – series microprocessor design team. He received his M.S and Ph.D from the EECS Department of University of Michigan at 2002 and 2004 respectively. From 2004 to 2012, Rahul was a research staff member at IBM T. J. Watson Research Center where he was been involved in the design and power reduction of IBM’s POWER processors as a member of the Advanced RISC Design Department. Rahul has served on technical program committees for ISLPED and VLSI Design and has also been the guest editor and review committees for several IEEE journals and conferences. He has presented several tutorials in recent years at ITC, IOLTS, VTS and IRPS. Rahul is a senior member of IEEE. His research interests lie in low power design, reliability and variability characterization – compensation systems, high performance memory and 3D design.

Sridhar Rangarajan received the B. Tech. (Hons.) degree in Computer Science and MSc. (Hons.) in Economics from BITS, Pilani and M.S. in Computer Science and Engineering from Santa Clara University USA. He has around 15 years of EDA experience leading various positions primarily in physical design domain. Currently at IBM, he is involved in leading the development effort of tools and methodologies for next generation microprocessors. Before joining IBM, he was working in Synopsys where he involved in developing the next generation router – zroute. He also held various technical positions in Sun, Monterey Design Systems and Cadence, involved in developing physical design tools and solutions. His research interests include CAD VLSI for physical design, routing, DFM, combinatorial optimization, graph algorithms.

Puneet Gupta is currently a faculty member of the Electrical Engineering Department at UCLA. He received his B.Tech from IIT Delhi in 2001 and Ph.D. in 2007 from University of California, San Diego. He co-founded Blaze DFM Inc. (acquired by Tela Inc.) in 2004 and served as its product architect till 2007. He has authored over 80 papers, 15 U.S. patents, and a book and a book chapter on topics at the design-manufacturing interface. He is a recipient of NSF CAREER award, IBM Faculty Award, ACM/SIGDA Outstanding New Faculty Award, EDAA Outstanding Dissertation Award, etc. Dr. Puneet Gupta has given several tutorial talks at conferences such as DAC, SPIE, ICCAD, ICMTS, etc. He has served as the Program Chair of IEEE DFM&Y Workshop 2009-2011 and is the director of the multi-university IMPACT+ center. His research interests lie at the design-manufacturing and hardware-software interfaces for improved cost, predictability and power/performance of integrated circuits and systems.