VLSI Design 2009
Technical Program Committee

Program Co-Chairs
Preeti Ranjan Panda, IIT Delhi, India
Rajendra Panda, Freescale Semiconductor, USA

Tracks (Names of Track Chairs or Co-Chairs are in BOLD)

AMS: Analog, RF, Mixed Signals
Shouri Chatterjee, IIT Delhi, India
Debapriya Sahu, Texas Instruments, India
G.S. Visweswaran, IIT Delhi, India
Nagendra Krishnapura, IIT Madras, India
Pavan K. Hanumolu, Oregon State University, USA
Prakash Easwaran, Cosmic Circuits, India
Sambuddha Bhattacharyya, Synopsys, India
Shanthi Pavan, IIT Madras, India
Srinivasan C, Cosmic Circuits, India
Vivek G. Pawar, Sankalp Semiconductor, India

ASA: Application Specific Architectures, Security
Nitin Chandrachoodan, IIT Madras, India
Sudeep Pasricha, Colorado State University, USA
Ashish Mathur, Freescale Semiconductor, India
Mona Mathur, ST Microelectronics, India
Sivakumar Sri, Wipro, India
Sri Parameswaran, UNSW, Australia
Sri Chandra, Freescale Semiconductor, India
Sriram R. Vangal, Intel, USA

PHY: Physical Design, DFM, Power and Signal Integrity, Interconnect and Timing Analysis/Optimization, Reliability
Puneet Gupta, UCLA, USA
Susmita Sur-Kolay, ISI Kolkata, USA
Chul-Hong Park, Samsung, S. Korea
Elaheh Bozorgzadeh, University of California, Irvine, USA
Florin Balasa, Southern Utah University, USA
Min Zhao, Magma Design Automation, USA
Murat Becer, CLK-DA, USA
Puneet Sharma, Freescale Semiconductor, USA
Sao-Jie Chen, National Taiwan University, Taiwan
Savithri Sundareswaran, Freescale Semiconductor, USA
Shabbir Batterywala, Synopsys, India
Vishal Khandelwal, Synopsys, USA
Vladimir Zolotov, IBM, USA
Kolin Paul, IIT Delhi, India
Tulika Mitra, National University of Singapore, Singapore
Anup Gangwar, AMD, India
Basant Dwivedi, Calypto Design Systems, India
Javier Resano, UCM Madrid, Spain
David Atienza, UCM Madrid, Spain
Madhu Mutyam, IIT Madras, India
Mahesh Mehdendale, Texas Instruments, India
Nikil Dutt, UC Irvine, USA
Niraj Jha, Princeton University, USA
Paolo Ienne, EPFL, Switzerland
Pradip Jha, Xilinx, USA
Samarjit Chakrabarty, National University of Singapore, Singapore
Sarma Vrudhula, Arizona State University, USA

LPE: Low Power Electronics
Nagi Naganathan, LSI Corp, USA
Praveen Elakkumanan, IBM, USA
Amit Patra, IIT Kharagpur, India
Bharadwaj Amrutur, IISc, India
Ram Krishnamurty, Intel, USA
Tezaswi Raja, LSI Corp, USA
Xin Li, CMU, USA
Aditya Bansal, IBM, USA
Saibal Mukhopadhyay, Georgia Tech., USA

TECH: Technology, Device Modeling and Simulation, MEMs, Nanoelectronics, and Biological Systems
Rajiv Joshi, IBM, USA
Bipul Paul, Toshiba, USA
Durgamadhab Misra, NJIT, USA
Josef Watts, IBM, USA
M. Jagadesh Kumar, IIT Delhi, India
Madabusi Govindarajan, IBM, India
Sukumar Jairam, Texas Instruments, India

ARCH: Processor Architecture, Multi-core Systems
Vijay Degalahal, Intel, India
Ashok Jagannathan, Intel, India
Maurizio Palesi, UNICT, Italy
Petru Eles, Linkoping Universitet, Sweden
Nagarajan Ranganathan, University of South Florida, USA
S.K. Nandy, IISc, India
Sourav Roy, Freescale Semiconductor, India
SYN: Design Specification, Modeling, and Synthesis, Hardware/Software Co-design, Simulation, Emulation and Formal Verification

Prabhat Mishra, University of Florida, USA
Indira Iyer, Synfora, India
Jayanta Bhadra, Freescale Semiconductor, USA
Logie Ramachandran, Synopsys, USA
Malay Haldar, Calypso Design Systems, India
Pallab Dasgupta, IIT Kharagpur, India
Saraju Mohanty, University of North Texas, USA
Shankar Hemmady, Synopsys, USA
Sandeep Shukla, Virginia Tech, USA

TEST: Testing, DFT
Srivaths Ravi, Texas Instruments, India
Adit Singh, Auburn University, USA
Bernard Courtois, CMP, France
Bhargav Bhattacharya, ISI Kolkata, India
Kartik Mohanram, Rice University, USA
Kewal Saluja, University of Wisconsin, USA
Nagesh Tamarapalli, AMD, India
Pradip Thaker, Analog Devices, India
C. P. Ravikumar, Texas Instruments, India
Rubin Parekhji, Texas Instruments, India
Srimat Chakradhar, NEC Labs, USA
Sudhakar Reddy, University of Iowa, USA
Vishwani Agrawal, Auburn University, USA