Tutorial T6

Negative Feedback System and Circuit Design

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Abstract

The negative feedback amplifier structure using an ideal integrator is derived. The time domain and frequency domain descriptions of the integrator are discussed. The response of the negative feedback amplifier in the time and frequency domains is analyzed. From these general conclusions are drawn about the behavior of negative feedback amplifiers.

The ideal integrator is realized using controlled sources and passive elements. This realization clearly shows the cause for finite dc gain in real opamps. The effects of finite dc gain are analyzed. Relationships between amplifier specifications such as speed and accuracy and opamp parameters such as unity gain frequency and dc gain are derived.

Methods of increasing the dc gain to improve accuracy are discussed. These lead to multistage amplifiers. The response of such systems in time and frequency domains are analyzed. It is shown that multistage amplifiers are potentially unstable. Stability conditions for negative feedback systems are discussed.

The gain around the negative feedback loop is computed. The significance of loop gain is illustrated. Stability criteria related to the loop gain such as phase margin and Nyquist’s criterion are discussed. Frequently used criteria such as phase margin are clarified.

Multistage amplifiers are essential for realizing high accuracy. Different techniques of realizing high gains while retaining stability-increasing the output resistance, miller compensation, and feedforward compensation are shown.

There are various opamp architectures: folded/telescopic cascode; two stage miller compensated; feedforward compensated; and three stage. The design procedures for the two stage miller compensated opamp, the feedforward compensated opamp, and the three stage opamp are shown. These opamps will be compared in terms of their performance parameters-bandwidth, noise, power dissipation, slew rate, output swing.

The design of a 350MHz bandwidth continuous-time active-RC filter using feedforward compensated opamps is shown. Measurement results from chips designed at IIT Madras illustrate the benefits of the feed-forward opamp architecture for low power applications.

The design details of a three stage opamp with a DC gain exceeding 100dB is shown. The constraints on the design of different stages are evaluated. Simulation results of the opamp illustrate its suitability for a high precision application.

Speaker Biographies

Nagendra Krishnapura is an Assistant Professor of Electrical Engineering at the Indian Institute of Technology, Madras in Chennai. He obtained the B.Tech degree in Electronics and Communication Engg from the Indian Institute of Technology, Madras in 1996 and the masters and doctoral degrees from Columbia University, New York in 1998 and 2000 respectively. Between 2000 and 2005, he worked as a senior design engineer at Celight, Inc. and Multilink (later Vitesse Semiconductor) where he designed integrated circuits for high speed broadband communications. Since June 2005, he has been with the Department of Electrical Engineering of
the Indian Institute of Technology Madras, where he teaches, conducts research and consults for several companies in the areas of high speed analog circuit design and signal processing. Nagendra has been an adjunct faculty member at Columbia University, New York, where he taught several advanced courses on analog design. He is also involved in improving expertise in the areas of analog and mixed signal design in India through the Prof. K. Radhakrishna Rao foundation. He and Dr. Shanthi Pavan presented a tutorial on continuous time delta sigma data converters at the VLSI conference in 2008. Nagendra Krishnapura is an associate editor of *IEEE Transactions on Circuits and Systems, Part II: Express Briefs*.

**Shanthi Pavan** is an Assistant Professor of Electrical Engineering at the Indian Institute of Technology, Madras in Chennai. He obtained the B.Tech degree in Electronics and Communication Engg from the Indian Institute of Technology, Madras in 1995 and the masters and doctoral degrees from Columbia University, New York in 1997 and 1999 respectively. From 1997 to 2000, he was with Texas Instruments in Warren, New Jersey, where he worked on high speed analog filters and data converters. From 2000 to June 2002, he worked on microwave ICs for data communication at Bigbear Networks in Sunnyvale, California. Since July 2002, he has been with the Department of Electrical Engineering of the Indian Institute of Technology Madras, where he teaches, conducts research and consults for several companies in the areas of high speed analog circuit design and signal processing. Shanthi Pavan serves on the editorial board of the *IEEE Transactions on Circuits and Systems, Part I: Regular Papers*. Apart from having taught several short courses in industries (like Texas Instruments, ST Microelectronics, National Semiconductor, Genesys Microsystems and many others), Shanthi has offered a tutorial on System Level Aspects of A/D Converter Design in the VLSI Design Conference in Hyderabad in 2006 and, with Nagendra Krishnapura, a tutorial on oversampled delta sigma data converters in 2008. He is also involved in improving expertise in the areas of analog and mixed signal design in India through the Prof. K. Radhakrishna Rao foundation.