Tutorial T5
Design for Manufacturability and Reliability in Nano Era

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Abstract
The bottom line of any company is to maximize the profit from any given product. There are many factors influencing the product design resulting in a profitable business. One of the biggest factors is the manufacturability of the product. It is becoming more and more crucial to meet the 6+6 (6 months for the development and 6 months for qualifying the product to ship to customer) product life cycle to accommodate the rapid changing technology hungry market demand. Smooth, reliable, and efficient product ramp through manufacturing is the key of success for meeting TTM, capturing higher percentage of total available market (TAM).

This tutorial is going to address the difficulties industries are facing today in designing manufacturing friendly highly complex giga-scale products in submicron technology. As we are heavily into deep submicron era, the error margin or the tolerance guard band is getting tighter and tighter with respect to the previous generation of fabrication process. On this note, it is important to pay attention to Design For Manufacturing (DFM) related issues early in the design cycle as oppose to later in the design. These include, however not limited to, all kinds debugging hooks in the design for easy debugging of billion of transistors in a given design, paying attention to manufacturing friendly physical design rules, making sure of adequate test coverage to toggle most of the design nodes, making sure optimal guard band is implemented for transistor degradation for the lifetime of the product, and last but not least, all reliability (ESD, EM/SH, LU, etc) related issues are resolved in pre-silicon design before Tape out. In the past, manufacturing issues were not given much attention; time has changed and designers must have to be more sensitive than ever before in addressing manufacturing related issues early in the design cycle.

In a nut shell, this tutorial will capture the must have knowledge for design engineers (irrespective of front-end or back-end) who are involved in high performance VLSI design, as DFM features moving upstream in the design cycle. Audience will walk out with a good understanding on how to integrate specific manufacturing concerns into a product’s design to obtain a product that is easier to manufacture with excellent overall quality in a shortest development time.

This tutorial covers the following main topics in detail:

1. **Introduction:**
   a. 6+6 product development strategy and overview
   b. Technology Trend of VLSI products in the current design environment
   c. Design trend (Power optimization, verification complexity)
   d. High volume manufacturability challenges, such as Cost of test, DPM, reliability issues

2. **DFT:**
   a. DFT strategy & planning
   b. Fault models
   c. DFT features in nanotechnology designs
   d. DFT Features for test cost optimization
   e. Special test structures
3. **Design for reliability:**
   a. FIT estimation for Design
   b. Design features for reliability improvement
   c. Design for Burn-in support
   d. Design for transistor degradation
   e. ESD for high speed IO
   f. EM/SH requirement and it’s verification

4. **Design for manufacturability:**
   a. Process and Layout interaction and specific guidelines to reduce manufacturing defect
   b. Manufacturing friendly design rules
   c. Opportunistic usage of special cells to improve design yield

5. **Post silicon Validation process for reliability and manufacturability:**
   a. Wafer and Package Test characterization
   b. ESD/EM/SH/BI validation
   c. HVM platform for DPM measurement
   d. Test flow optimization
   e. Test hole resolution process and DPM bucketing

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**Speaker Biographies**

**Goutam Debnath** received a M.S. in Physics from University of St Louis, Missouri, USA and a M.S. in Electrical Engineering from Southern Illinois University, Carbondale, USA. Goutam is in the board of Industry Advisory Council for Electrical and Computer Engineering Department of Southern Illinois University. Goutam is the Intel QPI Technology Execution lead (TXT) and Manufacturing Program Manager (MPM) in Server Platform Group (SPG). He has acted as a manager on various microprocessor designs focusing on design, design automation. He has done 15 Intel based desktop processors and 4 Xeon processor in last 17 years of Intel’s professional carrier. Goutam’s primary focus is on achieving higher manufacturing excellence and smooth enablement of QPI technology across the industry. Goutam has published and co-authored 9 technical papers in numerous conference including IEEE and VLSI conference. He has two USA patents on clock distribution in control logic blocks and shared power grid distribution respectively.

**Paul Thadikaran** received his Ph.D. in Computer Science from State University of New-York, Buffalo. He is currently a Principal Engineer at the Client Platform Architecture Group in Intel Corporation and focused on development of next generation client platform architecture. He has been involved in various aspects of design and test of previous four generations of Intel’s IA-32 CPU. He has managed design methodology development, CAD tool development and standard cell library development targeted for CPU designs for past seven years. His areas of interest include methods and algorithms for test VLSI design, test and platform architecture. Paul has published more than 20 papers in IEEE/Intel conferences and journals. He has also co-authored a book on $f_{max}$ Testing published by Kluwer Academic Press. Paul has refereed several IEEE and ACM journals such as *IEEE Transactions on CAD* and *ACM Transactions on Design Automation in Electronic Systems (TODAES)*. He has also offered tutorials on high performance design and test at various International and Intel audiences.