Driving Analog Mixed Signal Verification through Verilog-AMS

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Abstract:

The complexity of today’s SoCs and applications are driving the need for faster and more accurate mixed signal verification. Additionally the percentage of analog content in mixed-signal designs is increasing rapidly. This requires a change in mindset: no longer can the analog and digital modules be verified independently. For these reasons Accellera has been leading the development of the Verilog-AMS standard, to enable accurate mixed signal design verification of systems containing thousands of analog/digital interface connections. The presentation will discuss the recent language enhancements that have been driven by the Verilog-AMS technical committee, to make system level analysis of analog and mixed signal designs much more efficient and accurate.

Speaker Bio:

Sri has been associated with Freescale's analog & mixed signal internal tool development for the past 7 years. Currently he manages the internal tool development activities for Freescale Semiconductor in Noida, and his interests include power estimation and analysis at the system level. He has been actively driving the Verilog-AMS language development efforts for the past 4 years through his role as the technical chairperson of the AMS committee. Sri has worked for Freescale Semiconductor (formerly Motorola Inc) for 13 years, starting his career with MIEL Bangalore and has worked at the Austin and Adelaide development centers. Sri holds a Master of Engineering degree from the Indian Institute of Science, Bangalore.