Design Automation Standards the IP providers perspective

Dr. John Goodenough, ARM

Abstract:

Design chain standards are all ultimately aimed to make the task of the Design Integration and Manufacture of System on Chip Products more efficient, improving turn Around Time, and effective improving quality and yield. Dr Goodenough will outline the standardization activities in which ARM is currently involved {including those managed by Si2 Accellera, SPIRIT, JEDEC, Eclipse, OpenMax OpenGL} and their relevance to the issues of the IP supply chain. He will discuss types of standards an their impact on IP. The presentation will also focus on some of the challenges in managing viable standards to broad market acceptance and the consequent need for an integrated roadmap between various standardization activities to give maximum benefit and leverage to the final end customers.

Speaker Bio:

John Goodenough is Worldwide Director of Design Technology at ARM, responsible for all aspects of design methodology including support for ARM’s internal production flows and IP deployment and integration. In the latter role he works extensively with ARM’s design chain partners and customers. John began his career in electronics as a Sheffield University research fellow investigating novel VLSI signal processing architectures. He then co-founded Infinite Designs, a consulting house specializing in advanced ASIC and embedded system design methodologies. As a present board member of Si2 consortium, past board member of Accellera, OSCI and the VSIA alliance and a founding board member of the SPIRIT consortium John has a passionate interest in finding pragmatic approaches to improving quality and turn around time for System-SoC designs. Dr Goodenough has strategic oversight of all of ARMs design standards activities. Dr. Goodenough holds a B.Sc in Engineering Science from Durham University and a Ph.D in VLSI Design from Sheffield University.

Dr. Goodenough is currently active board member of Accellera, SPIRIT, Si2 and have accountability for ARMs activities in OSCI.Jedec.