Implementing the Best Processor Cores (Half Day)

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Abstract

It is well-known that varying architectural, technological and implementation aspects of embedded microprocessors, such as ARM, can produce widely differing performance and power specifications. Frequency specifications of high-end realizations are often nearly 2x-3x over vanilla flows. Power optimization techniques used in high-end processor designs have also been reported to have the potential to produce 3x-10x improvements in power over standard flows. This tutorial reviews high-end processor design challenges, techniques and presents state-of-the-art flows for implementing embedded processors. These techniques include processor and architecture selection, verification, selection of technology node/process, selection of macros, selection and optimization of standard cell libraries, design/architecture and power planning, advanced timing and power optimization, design closure, design integration, variability-tolerance, and design-for-manufacturability. The tutorial arms the audience with the best techniques, tools and methodologies to select and achieve the best Silicon for state-of-the-art embedded processors.

Speaker Biographies

Vamsi Boppana received the B.Tech (Hons) in computer science and engineering from the Indian Institute of Technology, Kharagpur, India, in 1993 and the M.S. and Ph.D. degrees from the department of electrical and computer engineering at the University of Illinois at Urbana-Champaign in 1995 and 1997, respectively. He is the Senior Director of Technology for Open-Silicon, Inc, a leading fabless ASIC vendor. Prior to Open-Silicon, Dr. Boppana was the Co-founder and Vice-President of Engineering of Zenasis Technologies, a VLSI design company creating leading-edge automated transistor-level optimization technologies. He has authored or co-authored over 40 technical papers and has six granted patents. He has served on the program committee and as a session chair for several computer-aided design and test conferences, including the International Conference on Computer-Aided Design. His current research interests include all aspects of VLSI design, test and verification. Dr. Boppana received the Indian Institute of Technology TCS Best Project Award in 1993, the University of Illinois Van Valkenburg Fellowship for demonstrated excellence in research in 1995, the Best Paper Award at the VLSI Test Symposium in 1997, and a Fujitsu Laboratories of America Intellectual Property Contribution Award in 1999.

Rahoul Varma BEng(Hons) MCIM graduated in Microelectronics System Design from Brunel University, UK in 1997 and has been with ARM Ltd (Cambridge, UK) for 10 years; Since mid-05 Rahoul has led a team of processor implementation engineers in ARM Bangalore. Before his arrival in India he was the technical lead of the architecture and development of a L2 Cache Controller for ARM11 based products. Rahoul has three patents in Cache design, Trace and Security. He earlier worked in the ARM SoC consultancy group and delivered 5 device level tape outs delivering in the areas from spec to layout. He was also involved in the foundry program where he was technically responsible for the addition of many productized ARM hard macros and silicon qualification projects.
S. Balajee graduated with a Masters degree in Computer Science from BITS, Pilani in 1991. He has been with Texas Instruments for the past fourteen years, contributing in various technical and management roles. He is currently responsible for the processors development group in Wireless India Design Team. Balajee was also elected as Senior Member Technical Staff in 2003.