Gateway to Chips: High Speed I/O Signalling and Interface (Full Day)

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Abstract

The design of inputs and outputs to integrated circuits has traditionally been a straightforward task involving procurement of a specification and its implementation. In the past few technology generations design and implementation of integrated circuit I/O’s have become much more complex. Just as Moore’s Law predicts that functions per chip will double every 1.5 – 2 years to keep up with consumer demand, there is a corresponding demand for processing electrical signals at progressively higher rates. The International Technology Roadmap for Semiconductors (ITRS) predicts the I/O bandwidth (Gb/s) for high performance ASICs to be 30 Gb/s by the year 2015. Adding to the complexity is the need to conform to a plethora of emerging I/O specifications and continued focus on reliability regarding Electro Static Discharge (ESD) and Simultaneous Switching Noise (SSN), and the circuit designer has about as much challenges as one can stand. This tutorial presents the techniques and methods employed to build a low power, high bandwidth, highly reliable I/O. It covers the popular signaling standards like LVDS, DDR, XAUI and PCI-Express. Also to be covered are concepts of ESD and Signal Integrity. This section of the tutorial will cover the origins of ESD failures in chips, circuit and layout guidelines to avoid ESD failures and ESD testing procedures. Finally, the tutorial will give a detailed architectural overview of various emerging I/O’s such as the DDR, LVDS, and the USB-PHY.

Speaker Biographies

Senthil N. Velu received a Bachelors degree in Electrical and Electronics Engineering from Madras University in 1998 and a M.S. degree in Electrical and Computer Engineering from North Carolina State University in 2002. He joined the Centre for Circuit and Systems Solutions at Carnegie Mellon University as a member of Research Staff in 2002. At Carnegie Mellon he was involved in building an analog automation tool to optimize multiple design objectives in PLL and ADC design. In 2004 he joined ARM Physical IP as Technical Lead of the Analog Mixed Signal – I/O Circuit Design Group. His thesis and subsequent research has involved design and optimization of analog / mixed signal circuits. He has authored and presented several papers in IEEE and RFIC conferences and journals on this topic. His work has received an Honorable Mention Award at the RFIC conference (2000). His currents interests include Analog circuit design automation and high speed interface circuit design.

Nidhir Kumar received a Bachelors degree in Electrical Engineering from Delhi University in 1997. He was involved in High Speed I/O design at S.T. Microelectronics between 1998 and 2000. Since 2000, he has been working extensively in the area of IO and mixed signal domain at ARM Physical IP. He was instrumental in leading the design teams of high speed IOs including DDR3 and GDDR3 at 1.6Gbps. He also has prior experience in PLL design. At ARM, he leads the design and development activities in high speed IO design.
**Rajan Verma** received a Bachelors degree in Electronics Engineering from Punjabi University. He joined Semiconductor Complex Limited, a govt. of India organization, and played a key role in design and development of several analog and mixed signal products. He also made a significant contribution in development of High speed data PHY's like USB2.0 and 10/100 Ethernet PHY. Currently he is working as senior design engineer at ARM and his current interests include analog and mixed signal design and high speed interface design.