

**Abstract**

Historically, transistor process variations have been studied in great detail. As interconnect becomes a significant portion of circuit performance, signal integrity, power integrity and chip reliability, study of interconnect process variations has gained increased importance. This paper provides a comprehensive overview of types and sources of all aspects interconnect process variations, including VIA, contact, metal, dielectric barriers and low-k dielectrics. Chemical Mechanical Polishing (CMP) induced variations and etch induced variations in metal topography are covered. Both systematic and random process variations are discussed. Impact of these interconnect process variations on RC delay, circuit delay, crosstalk noise, voltage drop and EM are discussed. Foundations for statistical parasitic extraction and results from correlation to silicon are discussed. Methods to determine intra-level/inter-level variations and their impact on potential circuit hazards are covered.

The objective of the tutorial is to:

- Provide the audience (designers, EDA developers, EDA R&D, application engineers and academia), a clear picture of DSM realities in 130nm/90nm/65nm technologies:
  - Fundamental process realities
  - How variations scale with technologies: 130nm -> 90nm -> 65nm (-> 45nm)
  - What is the impact of these effects on design
- Types and Sources of Variations
  - Systematic vs. random variations
    - Within die
    - Die-to-die
    - Center-to-edge
    - Wafer-to-wafer
    - Lot-to-lot and
    - Fab-to-fab
  - Selective Process Bias
  - Dummy Metal and dummy VIAs
- Silicon structures for measurement of interconnect variations
  - VIA and contacts
  - Resistance
  - Capacitance
    - Dummy metal structures
    - SRAM bit-cells
    - Custom routes
    - Realistic routes
- Statistical Parasitic Extraction
  - Accurate modeling of systematic variations
  - Validation of assumptions in normal and non-normal distributions
- Methods to analyze interconnect process variations
  - Inter-level and Intra-level variations
  - Impact of variations on RC delay, crosstalk, IR-drop, Clock-skew and Power
    - Methods to minimize the impact of interconnect process variations