Tutorial T3

Testing Embedded Cores and SOCs—DFT, ATPG and BIST Solutions

Rubin A. Parekhji
Texas Instruments, India
parekhji@ti.com

Abstract

This tutorial presents a range of design and test techniques and considerations for incorporating high level testability into high performance SOC designs, constructed using embedded cores. Different solutions are proposed around DFT, ATPG and BIST techniques, and their implementation explained from the design and test viewpoints, for different components of SOCs. Capabilities of test automation tools to aid such implementations are explained alongside. Finally, a framework for design planning to assist in test logic implementation and validation, to meet aggressive design cycle times, is presented.

The material for this tutorial is derived from several chips successfully designed in the DSP and Broadband Design Centres at Texas Instruments, Bangalore, (India). These devices have offered a rich variety of design and test challenges, in terms of both the specifications as well as the implementations. Several novel techniques have been developed to address them, and their success has depended as much on correct planning, as on their correct implementation. The essence of these techniques is presented in the tutorial, in a design independent way.

This tutorial discusses various problems in embedded core and SOC testing, and presents solutions based on well-known DFT, ATPG and BIST techniques. The need and methods for adapting conventional test techniques to address new challenges faced in SOC testing are explained. Amongst other things, the tutorial describes techniques for ATPG of systems using IP cores by employing a scan model, the need for various test modes and construction of a test I/O interface to support them, design techniques for at-speed testing using transition fault and path delay fault ATPG, design support for memory BIST for fault detection and repair, and design support for logic BIST and techniques for rapid timing convergence. All the above techniques will be explained along with practical implementation careabouts in an SOC context. Accompanying results and tradeoffs will also be presented. (The focus of the tutorial is digital logic testing. Testing of analog circuits will not be discussed).

This is an advanced tutorial intended for IP core developers, system design and test engineers, as well as design and test managers. Basic knowledge of VLSI testing and core based system design is desirable to understand the design and test techniques and tradeoffs to be discussed in the tutorial.

Rubin A. Parekhji has been with Texas Instruments (India) from 1996, in their DSP and Broadband Design Centres. He is presently a Project Manager and Senior Member of Technical Staff. His team works on different products and competency projects in various areas of VLSI testing, for different embedded core based systems and SOCs being designed in these centres. The presenter has a Ph.D. from IIT Mumbai (Bombay). His areas of interest include different topics in VLSI testing and design verification.