Tutorial T2

Design of Deep Sub-Micron CMOS Circuits

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Abstract
Scaling down of device sizes and supply voltage requires a commensurate scaling of transistor threshold voltage to maintain high performance. Such scaling leads to exponential increase in leakage current, decreased noise immunity for high speed circuits, and increased defects. In this tutorial we will present design and test techniques to combat these problems in the deep sub-micron regime for bulk, SOI and future technologies. We will consider the following issues in turn:

1. Device scaling and its impact on sub-threshold and gate leakage current, interconnects, and noise immunity
2. Low voltage circuit design under high intrinsic leakage, leakage monitoring and control techniques, effective transistor stacking, multi-threshold CMOS, dynamic threshold CMOS, SOI implications. Design of low leakage data-paths and caches.
3. SOI design – comparison with bulk, logic and memory design, asynchronous design
4. Copper, Low k, and impact of Low k on performance
5. Future technologies – Double gate fully depleted SOI, FIN FET, and 3-D SOI
6. Noise modeling and analysis for high-speed precharge-evaluate circuits such as domino. Noise tolerant circuit design styles: skewed CMOS, noise tolerant domino, layout styles for high noise immunity
7. Iddq testing of circuits with high intrinsic leakage: delta Iddq, two parameter tests. Idd waveform analysis

This course will be useful for VLSI design engineers, managers, technologists, students, professors who are actively involved in VLSI design or to those who need to spread their knowledge across multi-disciplines. The tutorial is also intended for those who would like to know new developments in this field.

Dr. Rajiv V. Joshi is a research staff member at IBM's Thomas J. Watson Research Center in Yorktown Heights, N.Y. Dr. Joshi received his Bachelor of Technology degree from the Indian Institute of Technology in Bombay, India; a Master of Science degree from the Massachusetts Institute of Technology in Cambridge, Massachusetts; and a PhD from Columbia University, in New York, New York. From 1981 to 1983, he worked at the research labs of GTE in Waltham, Massachusetts. He joined IBM Research in November 1983 as a research staff member working on VLSI design systems for the science and technology department. He worked on sub-0.5 micron CMOS, DRAM and SRAM technologies. He developed novel interconnect processes and structures for aluminum, tungsten and copper technologies which are widely used in memory and logic technologies at IBM and around the world. His circuit related work includes design of registers, register files, latches, physical design tools, and L1 and L2 CACHes and directories. He also worked on designs in SOI technology and published widely. His leadership role and his circuit and
technology contributions has recently helped to achieve 2 GHz SRAM which is widely reported in newspapers. Dr. Joshi has won 19 invention plateau achievement awards from IBM and won two patent portfolio awards for cross-licensing and utilization of his patents in IBM products (Copper, Tungsten interconnects) and has received 4 research division awards. He holds 42 U.S. patents in addition to several pending patents. He has authored or co-authored more than 90 research papers and given invited talks at several conferences. (The papers were related to device interconnect structures and design of Ultra Large Scale Integrated Circuits). He has given several tutorials related to Technology and SOI based VLSI designs at technology and VLSI design conferences. He received the Lewis Winner Award in 1992 for an outstanding paper he coauthored at the International Solid State Circuit Conference (A 2ns cycle and 4ns access 512 Kb ECL SRAM). He chaired an advanced interconnect conference sponsored by MRS and served as an editor of the proceedings as well as a guest editor of MRS bulletin. He is in the program committee of International Low Power Symp., VLSI design 2000, Int SOI conf. and in the executive committee of Advanced Interconnect Conf. He is a Fellow of IEEE and a "master inventor" at IBM Research.

Kaushik Roy is a Professor in the School of Electrical and Computer Engineering at Purdue University, West Lafayette, where he is also a Purdue University Faculty Scholar Professor. He received his Ph.D. from the University of Illinois at Urbana-Champaign in 1990. Before joining Purdue University, he worked on FPGAs and low-power circuits in the Semiconductor Process and Design Center (SPDC) of Texas Instruments, Dallas, for three years. Professor Roy is known for his contributions in the area of low-power design, VLSI testing, and FPGA design. He has published over 200 papers in refereed journals and conferences and has five patents. He has also co-written a book on Low Power Design which was published by John Wiley in February 2000. He was/is on the editorial board of IEEE Transactions on VLSI Systems, IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications and IEEE Design and Test Computers and has served on the program and steering committees of several conferences. He was the guest editor for a special issue on low-power design in the IEEE Design and Test of Computers in 1994 and the IEEE Transactions on VLSI Systems (June 2000). Professor Roy received the National Science Foundation CAREER development award in 1995, ATT/Lucent Foundation award in 1997, an IBM Faculty Partnership Award in 2000. He received best paper awards in 1997 IEEE International Test Conference and 2000 IEEE International Symposium on Quality of IC Design for his work on testing of deep submicron designs. Professor Roy’s research interests are in low-power electronics for portable computing and wireless communications, VLSI testing and diagnosis, built-in-self-test techniques, re-configurable computing, and FPGA’s. His research is funded by DARPA (PACC, MSP), NSF, Semiconductor Research Corporation, DARPA/MARCO Gigascale Silicon Research Center, IBM, Intel, HP, Lucent, and Rockwell Corporation. Professor Roy is a Fellow of IEEE.