Tutorial: System Level Testability Issues of Core Based System-on-a-Chip

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Testability issues of a core based system-on-a-chip (SOC) are identified and the various solutions available at the different stages of SOC evolution are discussed. It was found that a strategy at core level and system level is needed to achieve first time success of the core based SOC. The issues considered include area, power and delay overheads, Fault coverage, At speed test, Core transparency, Low cost testing techniques, System level test strategies, Low power dissipation during system level test, System level test scheduling and Test generation techniques for Hardware-Software systems. IDDQ testing at core level and system level are discussed and strategies to schedule are discussed. DSM specific testability issues are discussed and their incorporation at core level and system level are planned. A flow for the SOC testability at core and System level is proposed to address the above issues.

The core based system-on-a-chip (SOC) is the natural evolution of future hardware to gain time-to-market and lower cost-effective solution to present day requirements. The testability of such a system poses a challenge due to the following issues—area, delay and power overheads, fault coverage, need for at speed test, core transparency requirements, evolving low cost testing techniques, system level test strategies, low power dissipations during system level testing, system level test scheduling and test generation techniques for hardware-software systems. DSM specific testability issues and IDDQ testing are discussed at core level and system level. In this tutorial the various testability issues and their solutions are analyzed and a testability flow is proposed.

Recently there are lot of research papers published which address each of the above problems. One of the works addresses the early prediction of testability by analyzing behavioral specifications. At the behavioral level the functional properties of the design are explicitly captured and can be used to speed up testability analysis. These information are difficult to extract from a gate-level design. Fault identification capabilities are becoming increasingly important in modern designs, not only in support of design debugging methodologies, but also for the purpose of process characterization and yield enhancement. In an effort to address size and complexity considerations, hierarchical approaches have become the dominant strategy for testing modern designs. There are problems tackled at the RTL level that include core transparency, at-speed test, reduction of area, power and delay overheads. A combination of core level and system level testability issues are addressed for core based SOC. These efforts include the two level strategy of core level testability based on standards like VSIA, IEEE P1500 and a combination of traditional DFT and new approaches. There are also efforts to evaluate system level test cost, cost effective system level test strategies, system level test: characterization and improvement, system level test infrastructure design and test scheduling and an efficient and economic partitioning approach for testability. There are frameworks developed for testing core based SOC. Efforts are also made to develop a unified framework for design validation and manufacturing test. The problems of test generation technique for hardware/software systems are being addressed in the literature. In this tutorial a methodology for system level testability is proposed based on the issues addressed and solutions and algorithms available in the literature. The importance of various evolving standards and reusability are kept in mind while proposing the method.