Tutorial: IBM's Blue Logic Design Methodology-Circuits and Physical Design

Speakers

Ruchira Kamdar
*IBM, India*

Seetharam Gundurao
*IBM, India*

R. V. Joshi
*IBM, USA*

Tutorial Coordinator

N. S. Murty
*IBM, India*

As the dimensions of ULSI circuits shrink to 0.12 micron and below, to achieve the highest device performance and density many challenges are to be met in designing circuits with performance driven physical design and the wirability of sea of transistors of the order of 100 million. This particular tutorial intends to cover advances in technology, relevant circuit techniques, synthesis and physical design methodology.

First the tutorial will outline IBM's Blue Logic Design methodology. Then the front and back end device technologies, the role of Aluminum Vs Copper interconnections, the importance of low-k dielectrics and reliability limits will be discussed. Issues related to other emerging technologies such as Silicon on Insulator (SOI) will be highlighted. The circuit techniques involving dynamic and static design will be discussed. Then the tutorial will proceed with physical design primarily focusing on custom and synthesis based design. The course will emphasize synthesis based layout techniques.

A brief description of the different design challenges such as high gate densities, deep submicron effects, low power requirements and packaging challenges will be given.

The Physical Design Tutorial will cover the logic Design methodology for taking a high level design from spec to Silicon with emphasis on the physical design aspects. A brief description of I/O placement strategy will be discussed. An overview of ASIC methodology flow with special emphasis on test insertion, clock tree re-powering, static timing, layout preparation and final design checking will be given. The course will further elaborate the complete PD methodology flow and various techniques used to optimize timing and wireability of the design.

Various packaging design options will be described along with their pros and cons. The essential offerings such as the Peripheral I/O Architecture, the Area I/O Architecture and the I/O planning will be reviewed. The other topics described will involve post processing of netlist to convert edge triggered design into design for test compliant structures, repowering of the ideal clock nets etc. Clock planning, insertion of balanced clock re-powering network, mapping of D flip flops to full- scan latches, connecting
latches and compilables into scan chains, and inserting boundary scan structures will be explained along with their benefits.

A brief procedure for physical design will be explained with the help of a case study. The procedure involves static timing analysis on the gate level netlist and physical design compatibility checks. The netlist is then processed for physical design, floor planned by specifying the technology parameters, package and image being used. The clock and scan associated elements are identified for future processing. All the cells of the design are placed and timed using steiner estimates for the nets. The clock cells are placed optimally using an optimization tool followed by a static timing check. The power and ground routes and the wires are wired. After the completion of wiring, the static timing tool is used to do a timing check on the wired design. After the timing sign off, a number of checks are performed to make sure that there are no problems associated with the final netlist.

Ruchira Kamdar did her ME in Micro Electronics from BITS Pilani. She has got 5 yrs of industrial experience in Physical Design, Signal integrity of IBM AS400 Systems and full custom design. She has worked with IBM's latest .12 micron copper technology and .11 micron technology. Her interests include physical design of chips and methodology development.

Seetharam Gundurao received his Master of Technology degree in Electronics Design and Technology from Indian Institute of Science, Bangalore, India and Bachelor of Engineering degree in Electronics and Communication from Karnataka Regional Engineering College, Suratkal, India. He has been working in Hardware Design Group of IBM Bangalore for four years in the area of VLSI design and verification in IBM's CMOS5s6, and SA12E technology. Currently he is working on formal verification of modules of a processor which is being used in one of IBM's products. His interests include ASIC design and bus architectures. He has filed six patents in the field of RAMDACs and IBM's Processor Local Bus, an internal bus for S-o-Cs.

Rajiv Joshi received his Bachelor of Technology degree from the Indian Institute of Technology in Bombay, India; a Master of Science degree from the Massachusetts Institute of Technology in Cambridge, Massachusetts; and a PhD from Columbia University, in New York, New York. He holds 38 U.S. patents and has authored or co-authored more than 80 research papers and given invited talks at several conferences. He received the Lewis Winner Award in 1992 for an outstanding paper he coauthored at the International Solid State Circuit Conference (A 2ns cycle and 4ns access 512 Kb ECL SRAM). He chaired an advanced interconnect conference sponsored by MRS and served as an editor of the proceedings as well as a guest editor of MRS bulletin. He is a senior member of IEEE and a “master inventor” at IBM Research.

N. S. Murty received his doctorate in Microelectronics from EE Dept, IIT Bombay and an M.B.A. from IGNOU, Delhi. He has 17 years of industrial experience, 10 years in VLSI design and 7 years in wafer fabrication process R&D, IC reliability evaluation and failure analysis. Currently he is a Deputy General Manager in Hardware Design Group of IBM Bangalore leading teams working on front end design and verification of multi-million gate designs in 0.15 and 0.11micron, Cu metal processes of IBM for processor, storage and networking applications. His interests include design project management and business development.