Tutorial: Optimization and Analysis Techniques for the Deep Submicron Regime

Speakers

Noel Menezes
Intel Corporation, USA

Sachin Sapatnekar
University of Minnesota, USA

Organizer

Sachin Sapatnekar

Scaling in the deep submicron (DSM) regime has fundamentally altered the primary issues affecting VLSI design. The emergence of DSM-related problems has resulted in a proliferation of design techniques that attempt to alleviate these newer effects in current flows. However, future design methodologies would be required to undergo a paradigm shift to comprehensively address these problems. A few of these newer problems are listed below:

Logical-physical codesign is now essential with the great dependence between logic-level optimizations and the actual physical design.

Interconnect has become a vital bottleneck in the performance of a circuit.

Design styles using dynamic logic have emerged as major contenders in high-performance design as it is no longer adequate to use static CMOS as the workhorse of circuit design.

As VDD levels go down, problems due to noise and leakage power will become paramount.

The design of global supply networks and clock networks will become harder with the increased chip complexities, and are more vital to the correct functioning of the circuit.

To overcome these, a wide array of new solutions has been proposed in academia and industry. The objective of this tutorial is to summarize the large body of literature related to DSM design, and in particular, to provide the audience with a vision of the state-of-the-art in the area of logic level and interconnect optimizations as well as delay/noise modeling. With the great need for design tools to help tackle these problems, it is important for both the design world and the CAD world to acquire a complete understanding of the issues involved. We will present a description of the problems in DSM design and describe computer-aided design (CAD) strategies that are used to overcome them.

Throughout the tutorial, an emphasis will be placed on the relevance of the proposed techniques to system goals and their influence on design flow. A recurring theme of the tutorial will be discussion of the relative merits of different problem formulations and how the solutions relate to system goals.
Noel Menezes is currently the manager of the Performance Verification group at the Strategic CAD Labs of Intel Corporation where he performs research in delay/noise modeling, interconnect optimization, timing analysis, and clock/power issues. Most of his work has been applied in the context of a design methodology for high-performance microprocessors. Among his other interests are high-performance circuits and interconnect modeling.

He received the Ph.D. degree from the University of Texas at Austin in August 1995. During his graduate career he has performed internships at the IBM T.J. Watson Research Center (1991) and the IBM-Motorola Somerset Design Center (Summer 1994). He has published several papers in CAD-oriented conferences and journals on the topics listed above.

Sachin Sapatnekar received the Ph.D. degree from the University of Illinois at Urbana-Champaign in 1992. He was an Assistant Professor in the ECE Department at Iowa State University from 1992 to 1997, and is currently an Associate Professor of ECE at the University of Minnesota. He is a co-author of two books, Timing Analysis and Optimization of Sequential Circuits (Kluwer, 1998) and Design Automation for Timing-Driven Layout Synthesis (Kluwer, 1993). He has served on the program committees for several conferences and has been an Associate Editor of the IEEE Transactions on Circuits and Systems II. He is recipient of the NSF Career Award and best paper awards at DAC-97 and ICCD-98. His research interests include physical design, power, timing and simulation issues, and optimization algorithms.