A High-grained Traffic Prediction for Microseconds Power Control in Energy-aware Routers

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Abstract—Recently, as significant increase of Internet traffic, power consumption of ICT devices is growing dramatically. Energy-saving of routers is one of important problems in future networks. There are some studies to reduce the power consumption by adjusting routers’ performance according to the volume of incoming/outgoing traffic. In such routers high-grained and accurate prediction of future traffic is very important for controlling power savings. In this paper, we propose a traffic prediction method suitable for performance adjustable routers which achieves accurate traffic prediction in short-term. We discuss about the impacts of prediction parameters and their tuning methods, for accurate of prediction. Through trace-driven simulations with real traffic, we show that our prediction method can reduce up to 95% of power consumption without any packet loss.

Keywords—Routers; Energy-aware systems;

I. INTRODUCTION

Recent years Internet traffic continues to rise globally, driven by increasing use of multimedia web services such as video sharing, and spreading of bandwidth-hungry devices such as smartphones [1]. Network providers are required to replace network equipments to higher-performance ones to accommodate high volume of traffic. However, using high performance network devices leads to an explosive increase in the energy consumption in ISPs. According to [2], routers and network switches are most energy-consuming devices in all of network equipments. Accordingly, energy saving and green networking are becoming global-scale problems which must be solved urgently. For example, in Japan, it is reported that the estimate of energy consumption of routers will be 14% of all ICT devices’ consumption. Reducing energy consumption in routers is one of dominant factors for saving the energy in ICT infrastructure.

Nevertheless, the current router design is not energy-friendly. In ISPs, the network is designed to be able to serve peak-time traffic. However, actually the traffic volume is variable and completely different between at off-peak and at peak-time, that is, the most part of capacity of a network device is not used, and very large amount of energy goes to waste during off-peak time. From the viewpoint of global warming, it is crucial to develop routers that can adjust routers’ power consumption according to the actual volume of traffic.

The typical router consists of several components, which are selected based on the scale of network, or bandwidth demands. According to [3], line-cards and switching fabrics consume more than half of total power consumption in routers. In line-cards, extremely large amount of power is consumed by LSIs such as memory chips and packet processors. As above, it is key for development of energy-aware routers to consider how to reduce the energy consumption of such LSIs based on the volume of network traffic.

From above backgrounds, Sliced-Router Architecture is proposed in [4]. This architecture accomplishes saving power consumption in routers based on the traffic volume. Every functional component that consumes large energy is divided into a set of multiple sub-components called slices, and slices process packets in parallel and independently.

There also have been some studies on saving power consumption of network devices. M. Hidaka et al. proposed the method of saving power consumption of routers, which controls performance of router in granularity of hours or up to 24 hours (1 day) according to the statistics of traffic over a past month [5]. Furthermore, P. Mahadevan et al. accomplished saving-energy of network devices according to the volume of network traffic by changing link speed dynamically [6]. However, both of these techniques assumed that recovery time of equipment is slow (in seconds or in minutes). Thereby, these methods focused on saving energy based on long-term fluctuation of traffic, such as in hours or days.

By contrast, the target of Sliced Router Architecture is to control power consumption in milliseconds. In this architecture, energy saving is acted in LSIs which enables to control power consumption in milliseconds. The big challenge in energy-aware routers is to reduce power consumption with avoiding any performance degradation caused by power controls. Short-term traffic prediction is key issue to avoid performance degradation. We list the requirements of traffic
prediction of Sliced Router Architecture.

1) The predictor can predict the traffic volume in microsecond-order interval.
2) Since the predicted volume is rounded by the unit of capacity of single sliced component, prediction errors less than the slice capacity are acceptable.
3) The calculation time of prediction is sufficiently short to slice recovery time.
4) Minimizing the latency caused by power control should be taken into consideration.

For prediction of future traffic demand, there are studies proposed so far. However, these calculate methods are usually based on neural networks or wavelet techniques, which are heavyweight because of their calculation complexity. Some of these prediction methods have milliseconds to seconds of prediction interval [7][8], however, these prediction techniques are still insufficient for Sliced Router Architecture that can control in order of microseconds.

Therefore, we propose finer-grained traffic prediction method which can be applicable to Sliced Router Architecture. Our method uses moving average and moving standard deviation, thus accomplishes fast calculation of traffic volume prediction. To evaluate proposed method, we collect the real traffic traces from the gateway of campus network, and demonstrate savings of energy by simulation. We also discuss about prediction parameters, to obtain the most gain of energy reduction. Our result shows that proposed method can reduce up to 95% of power consumption with appropriate parameters.

The rest of the paper is organized as follows. We provide an outline of Sliced Router Architecture in Section II. We describe the proposed prediction method and their parameters in Section III. We show simulation results of power reduction by applying our method in Section IV. Finally we conclude this paper with future topics in Section V.

II. Sliced-Router Architecture

In this section, we describe the overview of Sliced-Router Architecture, and show how proposed prediction method is used in this architecture.

A. Overview

In Sliced Architecture, the functional component of equipment is divided into a set of equivalent components. Here we define slice as sub-component of the original component, whose capacity is more than (or equal to) the original performance divided by the number of slices. One or more slices run simultaneously in parallel so that the component can preserve the same performance as the original component. For instance, suppose to use four slices to achieve 40 Gb/s of performance, these sliced components can provide 10 Gb/s of performance, and provide 40 Gb/s by processing traffic in four slices in parallel. Fig. 1 shows this concept. As listed in [9], functional components that can be sliced in typical core routers are buffer chips such as RAMs and TCAMs contained in forwarding engine and switch fabric. In Sliced-Router Architecture, slices are controlled based on the volume of traffic, specifically, as many slices as required are powered-on, and others are stand-by for the sake of improving the energy efficiency according to the demand of traffic. Regardless the type of component, the same approach can be applied to all types of sliced component, where we need to decide the number of required slices based on the demand of traffic.

For the power control in Sliced Router, we define three power-states of slice as follows.

- **Active**: Slice runs normally and processes packets.
- **Hot Stand-by**: Slice doesn’t work to process packets, however, a small portion of power is needed to skip initialization (or refreshing) of LSI to realize a fast resume to Active state.
- **Cold Stand-by**: Slice is shutdown and power to the slices is completely off.

In these three states, only Active slices can process packets. A shortage of Active slices would cause serious incident such as packet losses, therefore Hot Stand-by and Cold Stand-by slices have to be activated as many as needed. By contrast, if there are Active slices which are no longer needed in case when the traffic goes down, the excess Active slices have to transit to Hot Stand-by or Cold Stand-by state. Fig. 2 summarizes power-states and transitions of slice. In this paper, we focused on RAMs and TCAMs as components to be sliced, which are necessary for processing packets. From Cold Stand-by to Active or Hot Stand-by, initialization phase is needed which includes flushing memories, storing initial information, and so on. On the other hand, in Hot Stand-by state only the clock signal is not supplied and power is provided continuously to keep all data in the memory chips of sliced component. Consequently, to resume Hot Stand-by slice to Active state, it is only required to resupply clock signal. Therefore, the resume time from Hot Stand-by to Active state is extremely short compared to the time from Cold Stand-by state. Table I compares the details of three states. Note that we assumed the transition time is zero from Active to Hot/Cold Stand-by, and from Hot Stand-by to Cold Stand-by because these transitions are simply powering off of the slice.

B. Controlling power states and traffic prediction

Fig. 3 shows the detail of power controls to slices this architecture. Below devices are key functions for power control.
• **Brigade device** is the buffer that absorbs the difference between the ingress speed and the egress speed. This buffer is deployed in case of occurrence of an error of traffic prediction. Using larger buffer size can allow larger prediction error without packet losses, however the latency of packet forwarding becomes longer. Hence, the buffer size should be decided based on tolerance of the latency.

• **Traffic Predictor** estimates future traffic by using statistic information of traffic in past, and utilization of Brigade Device. It calculates required number of Active or Hot Stand-by slices. In Traffic Predictor, Traffic Counter gathers byte counts of ingress traffic, and Prediction Calculator calculates prediction value using gathered byte counts by Traffic Counter.

• **Slice Controller** manages power-state of slices based on the information from Traffic Predictor. It sends shutdown or resume signals to slices if needed.

• **Slice Scheduler** forwards input packets to Active slices in parallel. Through there are various scheduling algorithms, we use simple round-robin without loss of generality.

In this architecture, each input packet is processed by following procedure.

1) The packet is first stored to Brigade Device.
2) Slice Scheduler forwards the packet to one of Active slices based on round-robin fashion.
3) Each slice processes the arrived packet.
4) Before output, the processed packets from slices are aggregated.

In this architecture, it is necessary to predict the volume of traffic fast and accurately so that Brigade Device can catch up all packets. Traffic Predictor that fulfills the requirements already mentioned in Section I accomplishes such prediction of the traffic.

### III. TRAFFIC PREDICTION METHOD

In this section, we describe proposed prediction method and its concrete calculation method.

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**Figure 2. Power-states of the slice and state transitions**

**Table 1**

<table>
<thead>
<tr>
<th>State</th>
<th>Memory operation</th>
<th>Keep in formation</th>
<th>Power consumes</th>
<th>Resume time to Active</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active</td>
<td>Yes</td>
<td>Yes</td>
<td>100%</td>
<td>-</td>
</tr>
<tr>
<td>Hot Stand-by</td>
<td>No</td>
<td>Yes</td>
<td>44%</td>
<td>1 µs</td>
</tr>
<tr>
<td>Cold Stand-by</td>
<td>No</td>
<td>No</td>
<td>0%</td>
<td>100 µs</td>
</tr>
</tbody>
</table>

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A. Overview

The operation of Traffic Predictor is divided into four phases: Phase 1: Count the volume of input traffic. Traffic Predictor measures ingress traffic of the router, and stores the information of this. Phase 2: Calculate the predicted volume of traffic. Traffic Predictor predicts volume of future traffic according to the information collected in Phase 1. Phase 3: Get the utilization of Brigade Device. Traffic Predictor calculates the performance that need to clear Brigade Device according to its buffer utilization at the time. Phase 4: Calculate the number of required slices. Traffic Predictor decides the router’s performance will be needed in the future according to the results of Phase 2 and 3, and reports the correspond number of slices to Slice Controller.

Fig. 4 shows the timing sequence of operations in Traffic Predictor. We define the interval of each phase as prediction interval $I_p$, buffer watching interval $I_b$, power state interval $I_s$, respectively. In this figure, we set each interval by the unit of $I_p$, i.e. $I_b = 2I_p$ and $I_s = I_p$. We also define the delay in calculation of prediction as $\Delta_b$, and the delay in transition of the slices as $\Delta_t$. In Phase 1 Traffic Predictor gathers the information of traffic in the range of $t = t_0$ to $t = t_0 + I_p$. Then in Phase 2 predicts the volume of traffic in range of $t = t_0 + I_p$ to $t_0 + I_p + \Delta_b$. In Phase 3 do nothing at $t = t_0 + I_p$ because we assumed $I_b = 2I_p$. Finally, in Phase 4 calculates the number of slices will be needed in the future in $t = t_0 + I_p + \Delta_t$. Due to the delays for calculation $\Delta_b$ and transition $\Delta_t$, there is also a delay in applying prediction after calculation of Phase 4 is completed. In this paper, we consider time $t$ as slotted time, and the interval of timeslot is equal to $I_p$. 

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**Figure 3. Power Controls in Sliced-Router Architecture**

**Figure 4. Sequence diagram of the Traffic Predictor**
to consider the mechanism to reduce the accumulated error in traffic prediction. In this paper, we adopt the method that watches the buffer utilization of Brigade Device periodically, and controls slices based on this utilization besides the traffic prediction. Hereinafter, we denote “watching buffer utilization of the Brigade Device” by simply “watching of the Brigade Device”. We define \( B_t \) as follows
\[
B_t = \begin{cases} 
  b_t \cdot \frac{I_p}{I_p} & \text{if } t = n \cdot \frac{I_p}{I_p} (n = 0, 1, 2, \ldots) \\
  B_{t-1} & \text{otherwise,}
\end{cases}
\]
where \( b_t \) is measured buffer occupancy (in bytes) at time \( t \). Thus, we redefine the Eq. 1 so that consider both prediction of the traffic volume and watching of the Brigade Device which is given by
\[
V_t = (P_t + B_t) + 2^\gamma E_t. 
\]

\[ B_t = \begin{cases} 
  b_t \cdot \frac{I_p}{I_p} & \text{if } t = n \cdot \frac{I_p}{I_p} (n = 0, 1, 2, \ldots) \\
  B_{t-1} & \text{otherwise,}
\end{cases} 
\]

\[ V_t = (P_t + B_t) + 2^\gamma E_t. \]

\[ B_t = \begin{cases} 
  b_t \cdot \frac{I_p}{I_p} & \text{if } t = n \cdot \frac{I_p}{I_p} (n = 0, 1, 2, \ldots) \\
  B_{t-1} & \text{otherwise,}
\end{cases} 
\]

\[ V_t = (P_t + B_t) + 2^\gamma E_t. \]
B. Metrics

We define two metrics for evaluating performance of proposed method, which are power usage and buffer usage of the Brigade Device. We define power usage as percentage of total consumed power of sliced components to non-sliced components which are always running Active state. For instance, if the power usage is 10%, we accomplish 90% reduction of power consumption. Thus, the lower power usage means reducing the more power consumed. Next, we consider the case when the number of predicted slices is less than needed, that is, the ingress traffic speed becomes higher than the egress. Since Brigade Device absorbs difference between the ingress and the egress traffic rates, the buffer usage of Brigade Device increases in such situation. Therefore, the lower buffer usage of Brigade Device means that the less traffic latency is accomplished. Below, the buffer usage of Brigade Device is simply denoted as buffer usage.

C. Tuning parameters

1) Tuning method: As we described in Section III, there are several parameters in Traffic Predictor. We need to discuss the parameters $\alpha$, $\beta$, $\gamma$, $I_p$, and $I_b$. In the following, watching interval $I_b$ is denoted by the coefficient of prediction interval $I_p$.

In this subsection, we use 1 min traffic trace that the highest utilization in whole traffic trace for tuning of parameters. The parameters are tuned in order of $\alpha$, $\beta$, $\gamma$, $I_p$, and $I_b$. First, we assign initial value to each parameter: $\alpha = 4$, $\beta = 4$, $\gamma = 2$, $I_p = 10 \mu s$, and $I_b = 256$. Next, we obtain results with $\alpha = 1$ to 10, but all other parameters are still set to initial values. After we obtain the appropriate value of $\alpha$, we obtain result with $\beta = 1$ to 10, but $\alpha$ is set to the appropriate value we now obtained, and all other parameters are still set to initial values. In this way, we also obtain the appropriate value of $\gamma$, $I_p$, and $I_b$. The criterion of this tuning is minimizing power usage under the condition that there is no packet-loss. Furthermore, to consider behavior of this architecture in various situations, we simulate variety of line utilization by varying capacity of router. In our simulation, we obtain the results with the utilization of 1% to 90%. We choose the buffer size of Brigade Device based on router capacity we now set. If we set router capacity to 10 Gbps, the buffer size of Brigade Device is set to 256 KB. In contrast, when we set capacity to 1 Gbps, we set the buffer size to 25.6 KB. In the evaluation in this paper, we assume that the number of slices of each component is 64.

2) Impacts of the parameters: In the following, we describe and discuss the impacts of the parameters: $\alpha$, $\beta$, $\gamma$, $I_p$, and $I_b$. Due to space limitation, we present only the result of 50% line utilization. Fig. 7 is plotted with power and buffer usage as the vertical axis and each parameter as the horizontal axis. The line with cross denotes power usage, and the bar denotes buffer usage. Additionally we plot the line utilization (50%) as solid line, which is ideal line of power usage.

First, we observe the impact of $\alpha$. The power usage increases as $\alpha$ increases with all of line utilizations. On the other hand, the buffer usage is minimized at $\alpha = 3$, 4. To avoid occurrence of packet losses due to buffer overflow, we set $\alpha$ to 3 as appropriate value.

Next, we discuss the impact of $\beta$. In most of line utilizations, the power usage increases as $\beta$ increases. However, this impact is ignorable small. On the other hand, the buffer usage is minimized at $\beta = 6$, 7. Therefore, we consider that the appropriate value of $\beta$ is 6.

Then, we observe the impact of $\gamma$. In most of line utilizations, the power usage increases as $\gamma$ increases, and buffer usage decreases as $\gamma$ increases. We observe significant increase in the buffer usage when $\gamma$ is set to 0. Therefore, we set $\gamma$ to 1 as appropriate value.

Next, we describe the impact of prediction interval $I_p$.

The power usage decreases as $I_p$ increases with all of line utilizations. On the other hand, the buffer usage is minimized at $I_p = 10 \mu s$. The impact when we set $I_p$ large is smaller on power usage, therefore, we set $I_p$ to 10 $\mu s$ as appropriate value.

Finally, we discuss the impact of watching interval $I_b$.

The power usage decreases as $I_b$ increases with all of line utilizations. However, this decrease is converged by $I_b = 256$. Besides, buffer usage increases as $I_b$ increases in all of line utilizations. Therefore, we consider that the appropriate value of $I_b$ is 256.

From the above, we determine the appropriate parameters: $\alpha = 3$, $\beta = 6$, $\gamma = 1$, $I_p = 10 \mu s$, and $I_b = 256$.

D. The effect on power-saving

To evaluate the performance of proposed method, we compare traffic fluctuations and power usage derived by traffic trace of 24 hours shown in Fig. 6. The result is shown in Fig. 8. This figure is plotted with power usage and line utilization as the vertical axis and time as the horizontal axis. The upper and lower line denotes power usage and line utilization, respectively. The result shows that power usage is follow up line utilization. Therefore our proposed method can achieve saving power consumption according to the volume of traffic. Furthermore, compared to components that always running Active state, the figure shows that our method reduces 95% of power consumption of components in off-peak hour.

We also show proportionality of power usage and the number of slices to the traffic volume using 1 min traffic trace same as used in Subsection IV-C. The result is shown
V. CONCLUSION

In this paper, we propose fine-grained traffic prediction method that absolutely necessary in Sliced Router Architecture for reduce the power consumption according to the volume of traffic. The proposed method achieves the calculation in microsecond-order by using moving average and moving standard deviation, moreover minimize the increase of traffic latency. We determine the appropriate parameters through the trace-driven simulations. Using these parameters, we show that our prediction method can reduce up to 95% of router’s power consumption in off-peak hours based on the volume of traffic without any packet loss. Future work includes discussion about spiky traffic, and mathematical consideration of the impacts of the parameters.

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