Performance Evaluation of the $\mu$ BTRON Bus

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Abstract

The $\mu$ BTRON bus is a simple yet fast LAN, used to connect electronic stationery goods to the BTRON workstations. The specifications of the $\mu$ BTRON bus feature fast real-time performance with the ability to transfer blocks of mass data at reasonably high speed, and cost effectiveness.

Yamaha has developed the LSI, called CML2, to implement the $\mu$ BTRON bus specifications. In order to confirm whether the CML2 met the expected performance requirements of the $\mu$ BTRON bus, a series of tests were made and the performance parameters were actually measured. In the tests, the CML2 was built on a VME board, where 68000 MPU controlled the CML2 LSI as well as carrying out some onboard test programs.

The result showed that CML2’s performance sufficiently met the original expectation of the $\mu$ BTRON bus specifications, by achieving a data transfer rate of up to 386 Kbytes per second, or a frame transfer rate of 10,490 frames per second maximum.

1 Introduction

The $\mu$ BTRON bus is a personal network that makes it possible to freely connect a variety of peripheral devices called electronic stationery goods to workstations that comply with the BTRON specifications. In a typical application, these electronic stationery goods are electronic pens, key boards, and printers.

However, the use of $\mu$ BTRON bus is not only intended to be applied to the BTRON workstations, but to other realtime oriented network applications such as electronic conference, musical instruments, studios, amusement systems, home controlling, and to factory automations. These realtime local area networks can of course become sub-networks of highly functional distributed systems (HFDS [3]). Table 1 shows some network parameters of these application examples.

In these realtime applications, obtaining a shortest possible transfer delay time becomes a crucial factor. In case of musical instrument application, for example, musician’s performing information on the keyboard should be transferred to, say, the sound generator connected elsewhere on the network with the transfer delay time of less than 1 msec. Also unlike the case of CSMA/CD, it is important to maintain such a transfer delay time to be predictable.

For this reason, the $\mu$ BTRON bus specification was designed based upon the token ring topology, but with modified protocol from that of existing token ring (IEEE802.5) [4]. To keep the transfer delay time of each frame in minimum, a frame length is limited to less than 136 bytes long. This ensures a frame of only few bytes in length can be transferred very quickly. And a large block of data of more than 136 bytes in length must be divided into multiple number of frames, each with 136 bytes maximum. Such frames can be treated as lower priority frames, and allow the insertion of higher prioritized frames in between. This split transfer function of large data chunk and prioritized insertion of smaller packets are handled in a MAC sub-layer.

Cost effectiveness, another important objective of the $\mu$ BTRON bus, is essential for this type of network to be used widely. Yamaha’s CML2 LSI was developed with intention to comply with the above objectives of the $\mu$ BTRON bus; realtime capability and the low cost.

This paper reports our evaluation of the performance on the CML2 LSI in detail. By doing this, the paper also describes the validity of the $\mu$ BTRON specification itself as the realtime local area network protocol.

2 Evaluation system

2.1 Hardware

The overall hardware configuration of the evaluation system is shown in Fig.1. The $\mu$ BTRON bus adapter board has two network connectors, so that a network ring can be constructed by linking the boards in series (without
Table 1 Characteristics of μBTRON bus application systems

<table>
<thead>
<tr>
<th>application system</th>
<th>number of nodes (typical)</th>
<th>required performance for mass data transfer</th>
<th>required real-time performance</th>
<th>used data length (typical)</th>
</tr>
</thead>
<tbody>
<tr>
<td>network for electronic stationery goods</td>
<td>2 - 10</td>
<td>1Mbps</td>
<td>&lt; 100msec</td>
<td>(various)</td>
</tr>
<tr>
<td>network for peripheral device sharing</td>
<td>5 - 20</td>
<td>over 1Mbps</td>
<td>&lt; 1sec</td>
<td>over 1Kbytes</td>
</tr>
<tr>
<td>electronic conference system</td>
<td>10 - 50</td>
<td>1Mbps</td>
<td>&lt; 100msec</td>
<td>a few bytes</td>
</tr>
<tr>
<td>network for musical instruments</td>
<td>10 - 30</td>
<td>1Mbps</td>
<td>&lt; 1msec</td>
<td>a few bytes and over 1Kbytes</td>
</tr>
<tr>
<td>LAN</td>
<td>10 - 100</td>
<td>over 1Mbps</td>
<td>&lt; 1sec</td>
<td>over 1Kbytes</td>
</tr>
<tr>
<td>home control system</td>
<td>50 - 100</td>
<td>1Kbps</td>
<td>&lt; 1sec</td>
<td>a few bytes</td>
</tr>
<tr>
<td>network for factory automation</td>
<td>20 - 100</td>
<td>1Mbps</td>
<td>&lt; 10msec</td>
<td>(various)</td>
</tr>
<tr>
<td>branch network of HFDS</td>
<td>50 -</td>
<td>1Mbps</td>
<td>&lt; 10msec</td>
<td>(various)</td>
</tr>
</tbody>
</table>

using a concentrator) as shown Fig. 1. The block diagram of the μBTRON bus adapter board is shown in Fig. 2. It is an intelligent board with CML2, 68000 MPU, ROM, and RAM. The CML2 performs basic frame transmission and reception control on a token ring. The MPU controls the CML2, conducts network management, communicates with the host computer board via VME bus, and may also be used to execute on-board application program by itself. The interface with a host computer is established through a large shared memory on the VME bus with a 2-level interruption.

Fig. 3 shows the set of specifications of the CML2. It is a random logic chip rather than internal processor based, and it features high speed operation and a small chip area. It also equips DMA logic on the chip between the data I/O registers and the data buffer area. This reduces significantly the load imposed on the MPU to carry out frame transmissions and receptions. Also the buffer areas which contain the data (to be transferred as frame) for transmission (or reception) can be chained to successively accomplish the DMA transfers with the CML2. With the help by software, a large chunk of data can be divided into multiple number of such frame buffers, and successively transferred.
MAC protocol: the μBTRON bus specification ver.1.0
signal speed: 4 Mbps
data transfer: 4 channel DMA built-in
  - real-time receive channel
  - real-time transmit channel
  - non-real-time receive channel
  - non-real-time transmit channel
Buffer chain function supported in each channel
ring signal clock: independent clock
HOST CPU: 16bit / 32bit CPU
package: 100pin QFP package
power supply: 5V

Fig.3. Characteristics of μBTRON bus communication control LSI (CML2)

2.2 Software

Fig.4 shows the configuration of the software modules resident on the μBTRON bus adapter board. It consists of a CML2 driver and a program used to evaluate the performance of the system. The driver controls the CML2 and executes the processes necessary to control and maintain the network. The evaluation program accesses the CML2 via the driver and measures the test parameters such as frame transmission rate and frame transmission delay time.

In order to decrease the software overhead, the evaluation program runs in the interrupt routine and calls appropriate drivers from within the interrupt routine. The drivers ensure re-entrancy and can be called from simultaneously running routines.

When measuring the frame transmission rate, test frame is successively transmitted within a specified time period. The frame rate and the data rate are then determined respectively by:

- frame rate = (total number of transmitted test frames / time period)
- data rate = (total number of transmitted bytes by test frames) / time period

The transmission delay is defined as a period from the timing that the frame transmission request issued to the CML2 driver until the timing when the transmission completion report is received. That is,

- transmission delay time = token wait time +
  - frame transmission time +
  - transmitted frame collection time +
  - token generation time +
  - CML2 driver process time

The performance evaluation program has a function to repeat this measurement and display the average value, the maximum value, the minimum value, and the distribution status of the transmission delay times.

3 Evaluation result

Major points of interest in the performance evaluation are depicted as following:
- Transmission rate
- Real-time capability
- Relationship between the number of stations and transmission delay times
- Throughput during high network load

The evaluation results for each of the above are shown below.

3.1 Transmission rate

Fig.5 and Fig.6 show the measured results of the data transmission rate and frame transmission rate, respectively. Tests were carried out over a network with no other load applied. Plot1 in Fig.5 shows the measured results of transmitting 1 frame at one time without the buffer chaining. Plots2 imply that buffer chaining would effectively increase the transmission rate. This is due to the fact that CML2's buffer chaining function is only one step software command and effectively reduced the software overhead.

When mass data is to be transferred, each frame should be chained and better carry the maximum length of 136 bytes. At this data length (136 bytes) with no chaining is enabled, a data transfer rate of 339 Kbytes/sec was obtained. With buffer chaining function enabled (10 buffers), the maximum data transfer rate of 386 Kbytes/sec was obtained (see Plot2).

When the μBTRON bus is applied to a network where control commands (e.g., MIDI events) are mostly transmitted, typical data length per transmission can be only a few bytes. In this case, how many frames are transferred at certain period of time becomes more important than how large a data chunk can be transferred by one data frame. Such network characteristics can be indicated by the number of transmitted frames per unit time. A transfer
rate of 4976 frames/sec was obtained at the data length of 8 bytes (with no buffer chaining, Plot4 of Fig.6). With buffer chaining function enabled (10 buffers), the maximum frame transfer rate of 10,490 frames/sec (8 bytes/frame) was obtained (see Plot5).

Plot4 shows, when the transmission data length is 20 bytes or less, the number of frames transmitted increases only slightly, even if the data length is shortened. This seems that the effect was saturated by a software overhead factor.

In Fig.5 and Fig.6, Plot3 and Plot6 show the theoretical limits of data transfer rate and frame transfer rate respectively. Two plots obtained by,

\[
\text{maximum frame transfer rate} = \frac{\text{signal speed}}{\text{data length} + \text{frame header length} + \text{frame trailer length} + \text{token preamble length} + \text{ring total delay length}}
\]

\[
\text{maximum data transfer rate} = \text{maximum frame transmission rate} \times \text{data length}
\]

From Plots 1, 2, 3, 4, 5, and 6, you can see that the performance is close to the theoretical maximum when using long frame lengths. As the data length decreases, the deviation from the theoretical maximum increases due to the software overhead factors.

3.2 Real-time performance

Fig.7, 8, and 9 show the results of the measurement of transmission delay time of frames (with higher priority and the data length of 8 bytes) under varying network traffic of lower prioritized frames. Fig.7 shows the result measured over a network with no other load applied. Fig.8 shows the result measured over a network with another station transmitting frames (with a lower priority and the data length of 136 bytes). Fig.9 shows the result measured over a network with 2 other stations transmitting the data frames (with a lower priority and the data length of 136 bytes).

According to the \( \mu \) BTRON bus priority control rule, a station with higher priority frames to sent makes a reservation for the next transmission when a token or a frame header passes through the station. Even in the worst case, this station will be able to transmit the frame no later than at most two other stations complete their transmissions (two frames). Since Fig.9 depicts the result of two other stations running, therefore, the transmission delay time of 836\( \mu \)sec in Fig.9 can be said to be the maximum delay time (the software overhead of about 100\( \mu \)sec is included in this value) of the network. Even if more than 3 stations

\[\text{Transfer delay test terminated.}\]
\[(\text{test condition})\]
\[\text{priority}=1\]
\[\text{frame length}(\text{INFOA8}(\text{byte})\text{ test times}=100000\]
\[\text{chain length}=1\]
\[\text{Destination address}=0x8002\]
\[\text{test result}\]
\[\text{average delay}=292(\text{micro-sec/frame})\]
\[\text{max delay}=492(\text{micro-sec/frame})\]
\[\text{min delay}=130(\text{micro-sec/frame})\]
\[\text{max delay}=(\text{micro-sec}) \times \text{times} \times \text{average delay}\]
\[\begin{array}{cc}
0 & 0 \\
100 & 292.5 \\
200 & 585 \\
300 & 877.5 \\
400 & 1170 \\
500 & 1462.5 \\
600 & 1755 \\
700 & 1947.5 \\
800 & 2140 \\
900 & 2332.5 \\
1000 & 2525 \\
1100 & 2717.5 \\
1200 & 2910 \\
1300 & 3102.5 \\
1400 & 3300 \\
1500 & 3497.5 \\
1600 & 3695 \\
1700 & 3892.5 \\
1800 & 4090 \\
1900 & 4287.5 \\
2000 & 4485 \\
2100 & 4682.5 \\
2200 & 4880 \\
2300 & 5077.5 \\
2400 & 5275 \\
2500 & 5472.5 \\
2600 & 5670 \\
2700 & 5867.5 \\
2800 & 6065 \\
2900 & 6262.5 \\
3000 & 6460 \\
3100 & 6657.5 \\
3200 & 6855 \\
3300 & 7052.5 \\
3400 & 7250 \\
3500 & 7447.5 \\
3600 & 7645 \\
3700 & 7842.5 \\
3800 & 8040 \\
3900 & 8237.5 \\
4000 & 8435 \\
\end{array}\]

Fig.7 Transmission Delay Time (when no load is applied)
are transmitting frames continuously, a higher priority frame is able to be transmitted within this delay time. In reality though, as the number of stations in the network increases, token circulation intervals become longer due to signal delay time of added stations. Thus the transmission delay time will increase by the factor of added signal delay. The signal delay time of a station is discussed in section 3.3.

### 3.3 Number of stations and transmission delay times

Table 2 shows the measured average transmission delay on the network under varying number of stations connected to it. In this measurement, 50 frames are transmitted at one time with the buffer chain function of the CML2. In this test, the measured transmission delay increases each time as the station is added. A 5 µsec increase of transmission delay is observed for each additional station. This can be said to be a signal delay caused by a processing of CML2 and the analog interface circuit.

<table>
<thead>
<tr>
<th>number of stations</th>
<th>average transmission delay time (µsec)</th>
<th>increased delay time (µsec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>338</td>
<td>-</td>
</tr>
<tr>
<td>2</td>
<td>343</td>
<td>5</td>
</tr>
<tr>
<td>3</td>
<td>348</td>
<td>5</td>
</tr>
</tbody>
</table>

(Measuring conditions : data length = 136 bytes, number of chained buffers = 50)

### 3.4 Throughput during high network loads

Table 3 shows the frame transmission rate of the network under varying frame priorities and number of transmitting stations. According to this table, when 2 stations are transmitting frames of a higher priority, another station can hardly transmit frames with a lower priority. It means that 2 stations can use up almost all transmission capacity of the network. If 3 stations transmit frames continuously (with the equal priority) at the same time, the network is said to be in an over loaded state. However, even at this overloaded state, notice that each station can still maintain high rate of data transmission.

<table>
<thead>
<tr>
<th>station 1 data transfer rate (Kbytes/sec)</th>
<th>station 2 data transfer rate (Kbytes/sec)</th>
<th>station 3 data transfer rate (Kbytes/sec)</th>
<th>total data transfer rate (Kbytes/sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>386 (priority=0)</td>
<td>201 (priority=0)</td>
<td>135 (priority=0)</td>
<td>402 (priority=0)</td>
</tr>
<tr>
<td>135 (priority=0)</td>
<td>135 (priority=0)</td>
<td>19 (priority=0)</td>
<td>340 (priority=0)</td>
</tr>
<tr>
<td>19 (priority=0)</td>
<td>19 (priority=0)</td>
<td>340 (priority=1)</td>
<td>378</td>
</tr>
<tr>
<td>386 (priority=1)</td>
<td>201 (priority=1)</td>
<td>135 (priority=1)</td>
<td>402</td>
</tr>
<tr>
<td>190 (priority=1)</td>
<td>190 (priority=1)</td>
<td>3 (priority=0)</td>
<td>383</td>
</tr>
<tr>
<td>135 (priority=1)</td>
<td>135 (priority=1)</td>
<td>340 (priority=2)</td>
<td>378</td>
</tr>
<tr>
<td>33 (priority=0)</td>
<td>325 (priority=1)</td>
<td>326 (priority=2)</td>
<td>358</td>
</tr>
<tr>
<td>1 (priority=0)</td>
<td>30 (priority=1)</td>
<td>326 (priority=2)</td>
<td>357</td>
</tr>
</tbody>
</table>

(Measuring conditions : data length = 136, number of chained buffers = 10)
The throughput is lowest when frames with different priorities are transmitted simultaneously. This throughput drop is due to the fact that the station wanting to free its high priority to the other stations has to temporarily preoccupy the network with its own cleanup procedure, consequently eating up the transmission capacity of the network by such overhead frames.

4 Summary

It seems that the above evaluation proves that the performance of the CML2, as well as the specifications of µBTRON bus protocol, is well within level where it can suffice for the requirements of real-time data transfer and, simultaneously, of sufficient amount of mass data transfer. It is also found that the network stays stable even under high load conditions, and that its behavior is predictable.

For actual file transfer, communication software is required to perform, among others, flow control and retry controls with the host of the MAC sub-layer (that was used in this evaluation). We are currently developing software for the LLC sub-layer and the transport layer in accordance with the µBTRON bus standards. This should enable, in the near future, the use of the µBTRON bus possible in ordinary office network usage.

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References


