Protocol Aware Test ..
It Has a Role, But Where? And How?

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This panel highlights the concern that existing ATE is falling short when it comes to mission-mode testing of devices with multi-functional capabilities, comprised of many cores. The complexity of SOCs is making it increasingly difficult to test with traditional test methodologies (e.g. complex inter-core interactions, with variable behavior, and asynchronous interfaces). This would seem to dictate that the traditional functional test architecture of today’s ATE is unable to adequately accommodate. Does the answer lie with investing more in device DFT or ATE functions?

Some key points to consider here:
- Structural validation vs mission mode emulation
- How to best exercise on-board instruments
- R&D investment in chips vs ATE
- General purpose ATE vs device specific
- Development by consortia vs competition

The architecture of semiconductor ATE has evolved significantly over the years in terms of performance, but the basic underlying methodology of deterministic test has remain unchanged. The continuing transition from functional test to structural test is based on the premise that, after design validation ATE simply needs to verify manufacturing process quality. Structural test did not demand significant change in ATE architecture, other than providing more optimal structural test performance at a dramatically lower cost.

Defining and developing Protocol Aware (PA) ATE on the other hand could be more of a revolutionary than evolutionary step for ATE architecture. For example, traditional pattern memory architectures would have to be augmented with high performance state machines. Minimizing pipelines to provide lower latency is a problem that may not be solvable. Defining the test program software requirements may be the most complex problem of all. One of the questions might be, does this really need to be a complete overhaul of the traditional ATE system architecture, or does the advent of the “Open Architecture” system facilitate development of focused spot PA solutions that can be integrated into exiting ATE architectures? Since the primary application of the Protocol Aware tester is in a mission mode testing, this would dictate that all components on the system work in some form of non-deterministic concert.

The issues involved with developing a new PA ATE architecture would be much more than just the technical challenges. The requirements definition for Protocol Aware tester would be a new precedent which would not have been market proven. The R&D expense for such a system could be quiet high and coupled with an unknown market and the market overlap with system testbenches – not likely.

To mitigate the technical and financial risk, an industry consortium might be one approach. The risk and development effort could be shared across many companies, both semiconductor and ATE. This was the model used by SEMATECH in the late 80’s to fund and develop advanced semiconductor fabrication technology (but with a little help from the U.S. treasury).

The resulting efficiency and cost of such an ATE system might be a concern. While the premise here is that the underlying test challenges have to be resolved, the PA tester could be relegated to a New Product Introduction (NPI) role. Since semiconductor technology is advancing at a much higher rate than ATE technology, it is reasonable to expect that it might be easier to develop more advanced mechanisms for the chip to test itself (e.g. DFT) than to rely on new external ATE capabilities. One example would be exercising on-board instruments through the JTAG port. This would not necessarily replace the role of the PA system in new product verification, rather would target high volume manufacturing test. However, to solve the issues being addressed by mission mode exercises, much more DFT research and development needs to be done. Several leading semiconductor companies are already deploying ad-hoc internal DFT methods to address the issues with inter-core communication.

In summary, the mission mode test issues need to be addressed, but the question is whether this will be in the form of more advanced DFT, the Protocol Aware Tester, or a hybrid solution.