COT Flow Imposes Added Requirements for Debug

Zahi Abuhamdeh
TranSwitch Corporation, Bedford MA 01730

NATURE OF COT DEBUG EFFORT
COT (Customer Owned Tooling) flow does require an added constraint on debug requirements. Third party IP is central to any COT strategy. A success or failure of a product hinges on the integrity of these IP blocks. In this context, IP can be any thing from gate level cells to hardened uProcessor cores. Even with perfectly robust screening criteria for the third party IP providers, integration issues, physical electrical interactions, application unique stresses on the block, can cause failures that have never been experienced in the Vendor’s test silicon.

Isolation, controllability and repeatability of IP Block level tests is very critical to working with 3rd Party vendors such that the problem can be contained and described. This effort has to be robust enough to the extent that the root cause of a failure is isolated to the block (or not) and the same situation be re-producible in the 3rd Party’s validation environment. Only then can 3rd Party vendors help in the debug and produce future enhancements on the IP.

To this end, both Design For Test (DFT) & Design For Debug (DFD) can work together to leverage one into the other since they have a lot in common. Nest I will discuss three techniques and approaches that help achieve both.

1) RE-USE OF PRODUCTION TESTS IN SYSTEM
Through the use of a bridge from the host on the system bus or the on chip uProcessor, we can directly control the JTAG TAP state machine. This gives us instant access to all production tests that are kicked off through the TAP. When a problem is suspected in certain blocks, we can quickly turn on Memory BIST or any specialized SerDes BIST that are part of the production tests. This has the advantage of being in the system and can validate outside of the Tester type environmental factors that only exist in the final application system.

This approach has been used to validate correct bring up of parts in-system.

2) IP ISSOLATION ON THE TESTER
Once an IP block is suspect, we try to isolate it further. Since our production tests include at-speed IP tests (we use combinations of BIST & functional vectors), Re-using them for debug is becoming more important. Since the IP is well defined, and we can very easily generate new stimulus to run at-speed. PLLs, SerDes and DDR interfaces fall into this category. When ever we encounter a functional problem, we quickly load the chip on the tester and generate a test that targets these areas to stresses them further. This helps us rule out the IP block for failures. This costs a bit more hardware to gain the flexibility in the at-speed test, but can be very important to quickly rule out all potential issues in the 3rd party IP.

3) PROCESS AND POWER INTEGRITY
A measure of operating environment of the blocks or 3rd Party IP is also critical. This involves a complete ‘health check’ of the silicon in-system. Clean supply designs and isolation practices help start on the right track. One problem is that they are tough to validate if they were done correctly once the silicon is built.

A new approach was developed through the use of on chip Ring Oscillators to identify Voltage/Temperature range of operation of the chip. This technique validates the voltage supply rails for integrity during production and later can isolate all variations attributed to the chips operating environment, be it on the tester, in the lab or in the customer site. This approach has helped identify bad sockets, poor power supply designs using this technique. It is also, relatively cheap to implement in silicon.

CONCLUSION
By augmenting production level IP centric tests with debugging hooks, a tremendous amount of leveraging can occur to justify the added debugging hardware. The physical foot print for the added debug capability will be small and the incremental design effort minimal. Experience has shown that these additions save the day enough times that they become standard practice with minimal upfront ROI justification.

FUTURE DIRECTION
Third Party providers need to pick and adopt an emerging standard or a technology platform that will allow production vectors (supplied by the vendor) to be used on the tester. Further more, to provide a high level interface that can generate specific debug sequences to help them identify failures in the IP Core. This same debug feature set, will also be available to the end user to allow similar tests in the system, were the application is running.