The IEEE 1149.1 boundary scan standard is over 16 years old and has proven to be an extremely useful standard for board level testing. The 1149.1 architecture consists of a TAP controller that provides access to test instruction and test data registers within an IC via a 4-pin interface. One of the most important features of the TAP is its protocol, which provides a simple and easy to use IC test interface. This protocol defines and enforces; (1) a Test Reset Mode, (2) a RunTest/Idle Mode, (3) an Instruction Scan Mode, and (4) a Data Scan Mode.

Additional IEEE standards that reuse the 1149.1 TAP based architecture include; IEEE 1149.4 (a Mixed Signal Test Bus Standard), IEEE 1149.6 (an Advanced Digital Interconnect Test Standard), IEEE 1532 (an In-System Programming Standard), IEEE 5001 (a Silicon Debug Standard) and IEEE 1500 (a Standard for Embedded Core Testing). Further, IEEE standards in progress that plan on reusing the 1149.1 TAP based architecture include; IEEE P1149.7 (a Standard for Reduced-pin and Enhanced-Functionality Test Access Port and Boundary Scan Architecture) and IEEE P1687 (a Standard for Access of Embedded Instrumentation).

The common thread that ties all these existing and future IEEE standards together is the TAP’s protocol and 4-pin interface. The following briefly describe how each of these additional IEEE standards extended the 1149.1 architecture into areas that it was not originally designed to support by the addition of pins, circuitry, instructions and procedures.

The IEEE 1149.4 standard took the 1149.1 TAP based architecture and added two analog test pins, instructions, circuitry and procedures for standardized use of the analog test pins to test and measure RLC elements within IC interconnects.

The IEEE 1149.6 standard took the 1149.1 TAP based architecture and added instructions, circuitry and procedures to allow standardized testing of AC coupled interconnects between ICs.

The IEEE 1532 standard took the 1149.1 TAP based architecture and added instructions, circuitry and procedures to allow standardized programming of circuitry within ICs.

The IEEE 5001 standard took the 1149.1 TAP based architecture and added additional pins, instructions, circuitry and procedures to allow standardized debugging of ICs.

The IEEE 1500 standard is based on the 1149.1 instruction and data register architecture but does not require using a TAP to access these registers. However, 1500 optionally allows use of a TAP to access its instruction and data registers if so desired.

The IEEE P1149.7 standard is taking the 1149.1 TAP based architecture and adding an interface adapter, protocols and procedures to enable standardized TAP access by either 2 or 4 pins during test and debug operations.

The IEEE P1687 standard is taking the 1149.1 TAP based architecture and adding additional pins, instructions, circuitry and procedures to enable standardized access to embedded test/debug instruments within ICs.

Since all the above 1149.1 based standards are controlled by the TAP interface, external controllers for accessing these test, debug and programming standards are simple to design and cost effective.

From the number of IEEE standards that have been and continue to be developed based upon the original IEEE 1149.1 architecture, it should be clear that the 1149.1 standard was “Built Right” and “Built to Last”.

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The IEEE P1687 standard is taking the 1149.1 TAP based architecture and adding additional pins, instructions, circuitry and procedures to enable standardized access to embedded test/debug instruments within ICs.

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