Role of Test in Yield Learning for 65 nm and Beyond

Thomas Ho
Credence Systems Corporation

1 Overview

Semiconductor test has been a component of yield learning since the beginning of the modern era. After all, finding faults in ICs and identifying their root causes is quintessential to yield improvement.

So what is new about this – new enough to warrant a panel discussion?

What is new was clearly stated at VTS 2005: “Test is becoming the only viable process monitor.”

As long as visible point defects dominated the failure pareto, inline inspections were effective in identifying most of the yield killers. In the nanometer era, however, this is no longer the case. Studies have shown that up to 80% of the defective devices fail because of process parameter excursions – and a significant part of the remaining 20% may be due to defects too small for light microscopes to image.

These facts gave rise to that ringing assertion, and this panel was convened to address it.

2 Test, Failures, and Yield Learning

What are these tortuous process issues?

The 180 nm technology node – the last of the “classical scaling” nodes defined by the ITRS – was reasonably easily brought on line. But it was clear even before many 180 nm products reached high volume that the next node – 130 nm – would be troublesome. This was due to the simple fact that the faster transistors at this node would not overcome the increasingly dominant effects of interconnect delay. So, in order to achieve the targeted speed increases, new materials had to be brought on line.

At the same time, the geometries imaged were well below the wavelength of the light used to image them, and diffraction limitations made their ominous debut. The progress of OPC in the past four years is awesome!

In today’s world, most DFT is scan-based, and the tools currently available are logic-based tools, using scan as the circuit access mechanism. But this is a big problem. Today, a large and growing proportion of the IC’s in the market are not completely digital.

“Test is the only viable process monitor.” So it was said, and so it is today. Test structures do not identify all the process weaknesses any more – indeed, neighbor-to-neighbor effects in high-density areas change the behavior of the individual circuit cells, so multiple examples of cells functioning beautifully in one area maybe fail in another, simply due to proximity effects combined with nominal process variation.

Cutting that tortuous 130 nm node geometry by half, and with extensive improvement in the OPC processes, we find ourselves today with a critical question: how do we find the process issues that are costing so much yield?

It is a three-way issue.

First, we have to identify, and locate, the flaw in the device that causes a failure. It may not be a “defect”, per se, because of the process issues already discussed.

Second we have to assure by careful analysis and reasoning that this flaw is in fact the root cause.

Third, we have to apprehend the changes in the process necessary to mitigate this flaw.

This three-way issue requires consistent – and continuous – interrelationships of three sharply different technologies – test, EDA, and PFA.

The role of test is to exhibit the manifestation of a circuit error that leads to a DUT failure. The role of EDA is to couple the manifestation with a location in the die. The role of PFA is to exhibit the physical structure of the circuitry in the neighborhood of the error so its cause can be apprehended clearly.

3 The SOC Challenge

Cell-phones, set-top boxes, iPods, and other consumer devices more and more dominate the marketplace. To focus simply on complex logic devices is insufficient. Yet the yield issue remains – and is perhaps even more serious because of consumer device cost pressures.
These mixed-signal and/or analog devices will not respond as effectively to scan-based tests. Yet the yield issues in nanometer technologies due to the lithography interactions previously mentioned remain.

Generally, in order to get acceptable precision in the analog circuits, minimal geometries are not so popular – as a consequence, it is to be expected that the proximity and OPC issues in the logic areas may not be so serious.

Yet it remains the case that, to get the most cost-effective circuit realization, it is necessary to make even precision analog circuits as small as possible (subject to the tracking and other precision requirements). So as the lithography technology continues to improve, OPC kinds of issues will inevitably appear.

As the EDA failure tools focus so strongly on logic tests based on DFT scan structures, techniques to locate and characterize the parametric circuit deviations in the analog cores in SOC devices must be pursued.

It is likely, then, that key approaches to circuit failure localization for subsequent physical failure analysis will continue to involve such techniques as emission imaging, LVP scans, and related circuit activity imaging techniques. For this reason, we expect that the emerging SOC devices will necessarily involve a very effective collaboration between fab, test, and design communities.

4 On-chip Instrumentation

Circuit complexity realizable at the 65 nm and below nodes enhances – nay, demands – the installation of proven cores (“IP”) with in-core testability features, particularly for lower-cost consumer devices with short market windows.

Emergent testability features include not just BIST, scan-based DFT, and logic compression for test data minimization, but also on-chip instruments focused on identifying IP core failures due to environmental issues such as temperature and voltage errors. It is urgently necessary for IP suppliers to be able to grasp quickly the reason that their proprietary cores do not satisfy their specifications in particular implementations, and the means to do this is more and more being incorporated in a variety of on-chip instruments. Indeed, there is current activity to create an IEEE standard to enable consistent installation of on-chip instruments – the IEEE P1687 IJTAG proposal.

Internal instrumentation – on-chip circuits that can report parametric deviations related to overall circuit operation – will ultimately be a rich additional resource to help determine the nature and root cause of circuit failures due to small parametric deviations. The connection between unexpectedly low VDD and marginal circuit design is but one of many kinds of examples we could imagine.

Capturing the measurements of such on-chip instrumentation and correlating them with the character of various systematic failures will be an insightful data mining activity – and adding to that activity the “classical” circuit activity imaging techniques so familiar to the failure analysis community gives further opportunity for effective yield learning.

5 Conclusions

The role of test in yield learning at 65 nm and below is manifestly much more significant than it had been in the “classical scaling” era of 180 nm and above.

The reasons for this are obvious:

- Inline inspections are hampered by lack of imaging resolution and high feature count.
- Upwards of 80% of device failures are due to process parametric deviations, rather than point defects – so there is nothing to see in an inline inspection step.
- Device complexity has so vastly increased that multiple-IP SOC’s have become “the way to go” for low-cost consumer devices such as single-chip cell phones.
- On-chip instrumentation used at final test provides internal environment measures that ATE captures and reports.