Self-checking CMOS circuit design

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Abstract
This paper presents a new technique for designing single stage fully complementary metal oxide semiconductor (FCMOS) and CMOS domino logic circuits so that they are totally self checking for all single breaks. It involves the encoding of the output of the circuit in an error detecting code. CMOS circuits designed using the technique have two outputs. Two of the combinations (01, 10) are considered to be valid code-words. The circuit is augmented such that any break in the modified circuit produces a non-valid output 11, thus ensuring automatic fault detection.

Introduction
As digital systems become more complex, the necessity to have systems that have the capability of self checking is growing. Self checking can be defined as the ability to verify automatically, whether there is any fault in the logic (chips, boards or assembled systems) without the need for externally applied test stimuli. Totally self checking circuits are very desirable for highly reliable digital system design, since all faults from a given set would cause a detectable, erroneous output.

CMOS has emerged as the dominant technology for manufacturing digital systems. A CMOS circuit consists of a P-network connected between Vdd and the output node, and a N-network connected between GND and the output node. The circuit for P-network and N-network bear a dual relationship by DeMorgan’s theorem. This type of CMOS circuits is known as FCMOS. An alternative method of designing CMOS circuits is to use the precharged principle. Such circuits are called CMOS domino logic circuits.

A CMOS domino logic circuit consists of a n-network for implementing the function and a clocked p-channel and a clocked n-channel transistor. Also a CMOS inverter is connected at the output to make it low during the precharge phase. The output node is precharged to 1 when the clock is low. During the evaluate phase i.e. when clock is high, if the input pattern closes the path between ground and output node, the output is pulled to 0 otherwise it stays at 1.

The realistic modeling of the defects in CMOS VLSI logic can be done only at the transistor level, since only at this level the complete circuit structure is known[1-3]. It has been established that breaks constitute significant portion of the defects occurring in CMOS circuits [4]. Breaks can be caused by either missing conducting material or extra insulating material [5]. Break defects in CMOS circuits can be of two kinds e.g. intra-gate breaks and signal line breaks. Fig.1 shows the possible breaks in an FCMOS circuit. Intra-gate breaks occur internal to a gate e.g. break in source line (S1), break in drain line (S2), break between p-network and output node (S3), break between n-network and output node (S4) or a break disconnecting both p-network and n-network from the output node(S5). Signal line breaks in FCMOS can either make the gate of only p-transistor (S6) or of a n-transistor (S7) float. It is also possible that gates of both transistor may float (S8) in which case one transistor may conduct and the other remain in a nonconducting state [6]. A break can be modeled by creating an open connection between the transistor’s source and drain.

Significant amount of research have been carried out in the area of testable CMOS designs [7-9], but not much have been reported on self-checking CMOS de-
A technique is presented in this paper for modifying CMOS circuits so that they will be totally self checking for all single break defects. It should be noted that in this paper we are considering only intra-gate breaks (S1-S5).

The following definitions describe the manner in which self checking circuits deal with faults [12].

**Definition 1:** A circuit is fault secure for a given set of faults, if for any fault in the set the circuit never produces an incorrect code word at the output for the input code space.

**Definition 2:** A circuit is self testing, if for every fault from a given set of faults, the circuit produces a non-code word at the output for at least one input code word.

**Definition 3:** A circuit is said to be totally self checking if it satisfies both the above properties i.e. it is both fault secure and self testing.

### Self checking implementation of CMOS domino logic circuits

In this section we present a new technique for making any single stage CMOS domino logic circuit totally self checking for all single breaks. The block diagram of the proposed self checking design for domino logic circuit is shown in Fig. 2. The original domino logic circuit has been augmented using three extra transistors, and an external input S which will be set to 1(0) if output F1F2=10 (01) has to be produced during normal operation. The output of the circuit is encoded in 1-out-of-2 code. A non-code word 11 at the output of the circuit indicates the presence of a fault in the circuit. For any break in a conducting path, both output lines F1 and F2 will assume a value of '1'. In Fig. 2 the circuit output F1/F2 are charged to 1 during the precharge phase i.e. when the clock is low. Once the clock CK goes high, outputs (F1/F2) will be code-words i.e. either '01' or '10' if there is no fault in the circuit. For any break in a conducting path in the circuit the outputs will remain at the non-code word 11.

**Lemma-1:** A CMOS domino logic circuit modified as shown in Fig. 2 is fault secure for all single breaks.

**Proof:** When an input pattern is applied to domino logic circuit, the circuit outputs F1/F2 are charged to 11 during the precharge phase i.e. when the clock is low. During the evaluate phase i.e. when clock CK goes high, either Vdd or Gnd is connected to the output node and set the output to 01 or 10 value. The output will only change to '01' or '10' if there is no break in the conducting path activated by an input pattern. If a path connecting Vdd (GND) to output node is activated and a break is present in the activated path, the output will remain at a non-code-word value 11. Since 11 is a non-code-word, the presence of the defect will be detected. Therefore, for any single break in the circuit the output is always set to a non-code-word value, and never to an incorrect code-word i.e. a 01 is not changed to 10 or vice versa. Hence the circuit is fault secure. QED

**Lemma-2:** A CMOS domino logic circuit modified as shown in Fig. 2 is self testing for all single breaks.

**Proof:** In domino logic there is just one conducting path from Vdd to output node. Therefore, the input pattern that connects Vdd to output node will be a test for a defect in that path. In other words in the presence of a defect the outputs will remain unchanged at 11. For a circuit with two or more conducting paths from GND to output node, it is possible that an input pattern may activate more than one conducting path from GND to output node. Therefore if a defect is present in one path, it might not be detected with such an input pattern. However, this does not mean that the defect is undetectable, because for each conducting path there exists a unique input pattern that enables only that path and disables all other paths from GND to output node. Such an input pattern will definitely set the outputs to a non-code-word value 11 in the presence of a defect in the conducting path. In other words there exists a test for each possible single break in a conducting path in the circuit; hence the circuit is self checking. QED.

To illustrate the proposed technique let us consider the domino CMOS circuit shown in Fig. 3 that implements the function \( F = AB + C(A + B) \). The augmented circuit is shown in Fig. 4. Consider a break at D1 or D2. When the input pattern \( S = 0, A = 0, B = 0, C = 0 \) is applied to the circuit, outputs F1/F2 will go to '01' if and only if there is no break in the activated path.

![Fig. 2 Block Diagram of Totally Self Checking Design of Domino CMOS Circuit](image-url)
otherwise they will remain at '11'.

Self checking design of FCMOS circuits

This section of the paper deals with the totally self checking design of FCMOS circuits. The block diagram of the proposed self checking design is shown in Fig. 5. The modification suggested in Fig. 5 for FCMOS circuit involves the addition of just six extra transistors, no additional input is required. As stated in the previous section, a non-codeword (11) at the output of the circuit indicates the presence of a defect in the circuit.

Lemma-4: Any FCMOS circuit augmented as shown in the Fig. 5 is fault secure for all single breaks in the circuit.

Proof: In the proposed design, when the circuit receives an input pattern and the clock is low, both outputs F1 and F2 are charged to 1. When the clock goes high, either Vdd or GND is connected to one of the output nodes. This results in discharging of the respective output node, thus producing 01 or 10 output. For any break in the path activated by an input pattern, the circuit will always produce F1=F2=1, a non-code output thus indicating the presence of a break. Since for any defect, the circuit never produces an incorrect code word i.e. 10 instead of 01 or vice versa, the circuit is fault secure for all single breaks. QED.

Lemma-5: Any FCMOS circuit augmented as shown in the Fig. 5 is self testing for all single breaks in a conducting path in the circuit.

Proof: In an FCMOS circuit, it is possible for an input pattern to activate more than one path from Vdd (GND) to output node. Therefore, if a defect is present in one of the paths it may remain undetected for such an input pattern. However, it can be easily verified that each distinct path from Vdd (GND) to output node has at least one unique input pattern that activates only that path and disables all other paths. Therefore, when such an input pattern is received, the break present in the activated path will manifest by producing a non-code value 11 at the output. Since for every possible break in a path there is at least one input pattern for which the resulting output is a non-code word, the circuit is self testing. QED.

As an example of the proposed technique let us consider the CMOS circuit shown in Fig. 6 that implements the function \( F = (A+B)(B+C)(C+\bar{A}) \). The self checking design of the circuit is shown in Fig. 7. In this circuit when the input pattern \( A=0 \ B=0 \ C=0 \) is received, all three conducting paths from Vdd to out-
input node are closed. Therefore if a break occurs in any of the paths, it will not be detected with this input pattern.

Similarly A=1 B=0 C=0 will activate the path with transistors T4 & T5 and hence will detect any break in this path. Let us consider a break at B4 (Fig. 7). When an input pattern such as: A=1, B=0, C=0 is received, and a break at B4 is present outputs F1/F2 will remain at non-codeword 1/1.

Conclusion

We have proposed a technique for designing CMOS circuits so that they are totally self-checking for all single breaks. This has been achieved by adding just a few transistors without affecting the speed of the circuit. In the circuits designed using the proposed technique all single breaks are detected automatically without applying any external test stimuli.

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References
