System Implementation of a 16-Kbps Waveform Coder Using Adaptive Vector Quantization

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ABSTRACT
The research of this paper presents the development of an Adaptive Vector Quantizer (AVQ) CODEC chip using Open Architecture Silicon Implementation System (OASIS) tools. The goal of this effort is development of a 16-Kbps AVQ coder prototype system which can be used as an alternative to the currently used 32-Kbps Adaptive Delta Pulse Code Modulation (ADPCM). The AVQ semi-custom chip layout uses 1.2 micron SCMOS technology and consists of over 157,000 transistors. The AVQ system is being designed with Mentor Graphics tools and is a 4-layer PC board encompassing over 50 analog and digital components.

INTRODUCTION
Recent advances in the computational capabilities of communication electronics have enabled more complex coding algorithms which typically need either large amounts of memory or increased computational capability as compared to traditional coding schemes. Due to the evolution of Application Specific Integrated Circuit (ASIC) chips, many of these new generation algorithms are within the realm of real-time capability and can be implemented on a single chip.

Vector Quantization (VQ) is a block coding technique which has been used for both source and waveform coding systems. Due to the vector coding nature of the coding algorithm, the VQ signal-to-noise ratio (SNR) performance is superior to scalar quantizers that are considered the benchmark standards for digital waveform coding. Although the VQ codebook works well within the trained data, outside-of-training-sequence tests can yield sub-par performance. Secondly, because of the fixed codebook quality of VQ systems, the hope for a universal codebook means using a training sequence of tremendous length containing all types of speakers. Even with a very long training sequence of data, there still could be non-typical sequences which will make the VQ SNR fall below acceptable levels. A method to adapt the codebook to the changing statistics of the waveform to eliminate the primary disadvantages of the VQ coding scheme is precisely what Adaptive Vector Quantization (AVQ) attempts to achieve. With the addition of a dynamically changing codebook algorithm, AVQ can be used as an universal coder.

ADVANTAGES
The AVQ coding algorithm offers several advantages over standard VQ. First, as with many adaptive schemes, the choice for the initial codebook is not critical to the steady state system performance. After a short transition period, the codebook adapts itself to the quantized version of the past L-input samples. This attribute eliminates the need for the computationally intensive codebook design algorithm used with standard VQ. Secondly, the AVQ coding process can adapt to different types of signals. This adaptation process is very similar to ADM or ADPCM scalar systems. In fact AVQ can be interpreted as a vector implementation of ADPCM. Thirdly, due to the decrease in computational load, AVQ can be more easily implemented via ASIC chips in a real-time system. This feature may make AVQ systems attractive towards standard digital coding networks. Extensive simulations and listening tests show promising results of AVQ performance for different vector sizes.
The AVQ ASIC is designed to satisfy both the encoding and decoding requirements. The chip architecture is depicted in Figure 2.

In order to allow for the possibility of future implementations using larger dimension sizes and lower bit rates, 8 chips are used in parallel for the encoding process. Each AVQ chip, when used as an encoder, reads the input and codewords and computes a 16-dimensional 8-bit uLaw (13-bit uniform) distortion to find the closest past vector. Inherent to this calculation is the adaptive error process, which is found by computing an average amplitude of past samples. The binary representation of the error bits and the index of the closest codeword are stored for transmission once all computations are complete. The transmission synchronization is handled by the control box. When the AVQ chip is used as decoder, it reads in 16 bits to describe the address of the closest vector and 16-bit to describe the quantized quantized error to reconstruct the signal.

VLSI IMPLEMENTATION
Open Architecture Silicon Implementation System (OASIS) CAD tools developed by Microelectronic Center of North Carolina (MCNC) were used for specifications, synthesis, simulations, and automatic layout of the ASIC AVQ. Design intent is captured with Logic-III and manual design layout is performed with Magic. VPR is used for automatic design layout, and simulation is performed with LDVSIM and CAzM. Logical and optimal non-overlapping two phase with on chip feedback clocking methodology is used. The chip is designed in 1.2 micron SCMOS double metal process, and as an 84-pin PLCC component operating at 5V. Chip size is 9.49 x 9.49 mm and contains 157,191 transistors. The chip layout will be shown.

The goal of the AVQ system development effort is to design a 16-Kbps serial transmission CODEC board. Two sections, an encoder and a decoder, will contain all necessary circuitry to transmit and receive analog voice signals band limited to 3.2 KHz. The encoding system is shown in Figure 3, while the decoding system is shown on Figure 4. For the encoding system the analog input signal is first filtered, sampled and quantized through a uLaw CODEC chip. The 8-bit uLaw samples are sent, at the same time, to all of the AVQ ASIC chips at the rate of 8000 inputs per second. Each AVQ chip
computes all necessary AVQ operations, reading in the codeword data (or the quantized past) through its corresponding 8Kx8 SRAM. A ROM is required for system startup. Each AVQ chip, at the end of its codebook, sends out its minimum distortion value to the controller (PLD) which in turn selects the chip with the ultimate codeword that will update the entire codebook and send out its index and error bits through the UART. Instead of designing a separate 16 Kbps channel, the decision was made to use a standard UART with a RS 232 Line. This decision insured an effective transmission rate without concern of creating a new synchronization scheme.

FUTURE DESIGN
The current AVQ chip has been fully simulated and ready for fabrication. The first operational prototype system is expected during late Spring 1992. Development is currently underway to design the next generation AVQ system - AVQ2. This system will contain all memory, A/D and D/A operations and control on a single chip. The chip architecture for AVQ2 is shown in Figure 5.

CONCLUSIONS
A complete 16-Kbps Adaptive Vector Quantizer was presented as a waveform coding system. OASIS CAD tools are used for specifications, synthesis, simulations, and automatic layout of the AVQ Codec ASIC chip. The ASIC chip has the following parameters: over 157,000 transistors, 1.2 SC MOS technology, 9.49 x 9.49 mm, clock frequencies of 8 KHz and 20 MHz, 84-pin PLCC package, and operating at 5V. A complete 16-Kbps AVQ Codec board is being designed and verified using Apollo workstation with Mentor Graphics software.
REFERENCES


331