CALLAS/OASIS: Combining Behavioral and Register-Transfer Synthesis Systems

Michael Pilsl
Siemens AG, Central Research Labs
Munich, Germany

Franc Brglez
MCNC, Center for Microelectronics
Research Triangle Park, N.C., U.S.A.

Abstract

While behavioral synthesis has still to prove its feasibility in an industrial environment, register-transfer level synthesis is already accepted. Especially, behavioral synthesis has to compete with state of the art register-transfer synthesis in terms of area and timing of the synthesized chips. We have performed several controlled benchmark experiments, using test examples and chip designs that range from 300 to 50,000 transistors. Our results demonstrate that behavioral synthesis can generate logic and layout with performance which is comparable to those produced from register-transfer descriptions provided by a designer.

1 Introduction

Given a behavioral specification of a digital system, the goal of synthesis is to produce a hardware that implements the behavior while meeting various design constraints, e.g. cycle-time, area, power etc. Two major tasks of synthesis are: (1) optimization of scheduling and resource allocation, resulting in a register-transfer description, (2) logic and layout synthesis, producing a final design representation that maps to efficient hardware. Often, both tasks are performed independently, without considering the trade-off and interaction between them. In this work, we combine both tasks into one by matching the interfaces between two systems: CALLAS [1] and OASIS [2].CALLAS transforms a VHDL-based behavioral description into an optimized register-transfer description. OASIS expands the register-transfer description to required data-path components, synthesizes all control specifications, performs global optimization by redundancy removal and submits the final standard cell netlist for automatic placement and routing. Integration of the complete synthesis process offers quick evaluation of trade-offs associated with different optimization strategies. Our benchmarks are based on several test examples and chip designs, ranging from 300 to 50,000 transistors, that were already synthesized with OASIS from a register-transfer description generated by a designer. Starting with the VHDL behavioral description as an input to CALLAS, we automatically produce a register-transfer description as an input to OASIS and then synthesize the logic and the final layout. The current results, with all benchmarks are consistent and encouraging: behavioral specification is more concise, easier to understand, and takes less time to write than the corresponding register-transfer description. Moreover, synthesis from the automatically generated register-transfer descriptions has generated logic and layout with comparable performance to those produced from the register-transfer description provided by a designer. The presentation is organized as follows. We begin with a short overview of the two systems, CALLAS and OASIS, following with an outline of the key objectives of our benchmark experiments. After describing one of the benchmarks in more detail, we discuss the status of experiment results and present conclusions.

2 A view of the CALLAS system

A VHDL-based behavioral specification [3] is the top-level design entry for the CALLAS system. The VHDL compiler translates this specification into a flowgraph which represents the sequence of all operations and the data dependencies in the VHDL program. Behavioral synthesis performs scheduling and allocation of all operations in the flowgraph. The objective of the currently used strategy is to synthesize a maximally parallel implementation of all operations in order to minimize the number of control steps for the
given algorithm. The underlying target architecture is a fully synchronous circuit consisting of a data path and a control unit. The data path is based on a multiplexor architecture. In addition, many optimizations can be performed on the synthesized register-transfer structure, e.g., register sharing, operator sharing, multiplexor minimization [4], and so on. A view of the CALLAS system in the context of matching its output to the top-level design entry of OASIS is shown in Figure 1. The OASIS interface that has been added to CALLAS produces a register-transfer description in the Logic3 language, using the components which are described in the abstract component library. Each element of this library is also specified by a Logic3 model for OASIS. Unlike in the traditional application of OASIS, no designer input is necessary to generate the required register transfer description to be compiled by OASIS into a layout of standard cells as described next.

3 A View of the OASIS System

OASIS is a cell-based design system with four major components: the compiler and logic synthesizer, the simulator and verifier, the automatic test pattern generator, and the automatic layout generator. Currently, the design is captured in Logic3, a PASCAL-like programming language that combines both functional and structural register-transfer descriptions. The functional description specifies finite state machines and decoding logic that can be readily synthesized into circuit structures by way of logic synthesis. A scan-path can be inserted automatically in every synthesized component. Data path circuits are synthesized hierarchically from parameterized structural/functional descriptions of subcomponents. Tools for redundancy identification can be used to detect and to remove any untestable logic. Following the design verification, test generation tools determine the fault coverage at the gate-level. Automatic standard cell placement and routing are performed after the circuit meets the design specifications. The final performance verification is based on the circuit extracted from mask data. The top-level flow chart of OASIS is shown in Figure 2.

4 Key Objectives of the CALLAS-OASIS Collaboration

MCNC design community includes full-time designers, faculty researchers from participating universities as well as graduate students. OASIS has been used to design several ASICs that were manufactured and performed correctly. The designs were complex and architecturally diverse: the applications included biomedical and speech processing systems as well as a ray-casting computer. Automated synthesis from register-transfer descriptions to standard cell layout has reduced the design time to months. The availability of behavioral specification and the designer-generated register-transfer description for each of these ASICs
makes them ideal candidates to benchmark the combined behavioral/register-transfer synthesis approach, using the CALLAS/OASIS interface as described earlier. As shown in Figure 3, a fair comparison of both approaches can be accomplished by comparing the final layout and performance of each design. We first considered the QRS and FAN chips with well-defined biomedical applications [5, 6, 7, 8]. To our knowledge, these are the first ASICs of significant complexity that have been synthesized automatically from a VHDL behavioral description all the way to standard cell layout and have been compared to the results of register-transfer synthesis. The compilation sequence itself can be accomplished within a day on a modern workstation.

5 The QRS Chip

The QRS chip [5, 6] has a biomedical application and is part of a real-time heart rate monitor. The algorithm implemented by the chip detects the QRS complex of an ECG as illustrated in Figure 4. The chip was designed using the OASIS system with its register-transfer synthesis capabilities. Considerable effort was initially required to optimize the QRS detection algorithm itself, resulting in a C-program that verified the functionality of the algorithm. In fact, rewriting the C-program in VHDL provided the first starting point for the behavioral synthesis. However, additional information has been added, to match the functionality of the real design.

6 Results

Table 1 summarizes the total number of transistors that are produced by the two approaches for each of the designs. The first two examples represent simple test cases, the FAN and QRS examples are biomedical applications. Notably, transistor count is comparable or even better than one generated from a register transfer description produced by the designer. All figures in Table 1 are based on 2.0μm scalable CMOS standard cell library. The synthesized results of the first two examples has been validated on gate-level, using the simulator of the OASIS system. The correctness of the VHDL-description of the QRS benchmark has been validated by a commercial VHDL simulator and compared to the results of the C-program.
Table 1: Synthesis from behavioral specification compared to register-transfer synthesis

<table>
<thead>
<tr>
<th>Circuit</th>
<th>OASIS Design Entry: Compiling Designer-Generated RTL Description</th>
<th>CALLAS / OASIS Design Entry: Compiling Designer-Generated Behavioral Description (RTL description generated by CALLAS)</th>
<th>Size in number of transistors</th>
<th>Size in number of transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Traffic C'ller</td>
<td>294</td>
<td>246</td>
<td>294</td>
<td>246</td>
</tr>
<tr>
<td>Display C'ller</td>
<td>804</td>
<td>774</td>
<td>804</td>
<td>774</td>
</tr>
<tr>
<td>QRS Chip</td>
<td>45,000*</td>
<td>38,694</td>
<td>45,000*</td>
<td>38,694</td>
</tr>
<tr>
<td>FAN Chip</td>
<td>56,800</td>
<td>51,990</td>
<td>56,800</td>
<td>51,990</td>
</tr>
</tbody>
</table>

*Includes about 6400 transistors for BIST circuit

Validation of synthesized designs, including layouts of both FAN and QRS chips, is still in progress and will be reported at the conference.

Testability of synthesized designs is of practical concern. Our initial results, before applying redundancy identification and removal, are shown in Table 2. The fault coverage of the synthesized design is surprisingly high, considering that current methods to include testability issues at behavioral level are far from mature. The relatively high coverage achieved for these designs points out that the design partitions, each synthesized to be 100% testable by OASIS, did not introduce signal reconvergence in ways that would affect fault coverage to a large degree. Proving the faults redundant provides additional opportunity to prune the logic and make the final design 100% testable. However, despite the high fault coverage for the initial circuits, the task of redundancy identification and removal is still CPU-intensive for the larger chip designs. As more and larger designs are synthesized from behavioral description, it will be essential that algorithms that implement redundancy identification continue to improve.

7 Conclusions

Several goals of this collaborative research project have been accomplished, including:

- A pragmatic and user-transparent interface which matches the register-transfer output of CALLAS to the register-transfer input of OASIS.

- Automatic generation of register-transfer description for OASIS from the behavioral VHDL-based description in CALLAS.

- Thorough verification of the combined CALLAS-OASIS compilation sequence, from VHDL-specification to standard cell layout, using a progression of diversified test cases and complex chip designs.

- Benchmarking combined behavioral/register-transfer synthesis versus synthesis from the designer-specified register-transfer specification, demonstrating significant potential for increased productivity as well as improved layout and performance by using the combined approach.

The following items are planned for future work:

- A release of the VHDL-descriptions for the benchmark set of the International High-Level Synthesis Workshop, including simulation patterns to enable validation of the synthesized circuits.
• Completing the validation process for the QRS and FAN examples.

• Application of the benchmark experiments to other scheduling and allocation strategies, to be integrated into the CALLAS system.

• Comprehensive report on all of the benchmark experiments to date [9].

8 Acknowledgement

This collaborative project has been supported by management and staff at Siemens and MCNC. The project would not have succeeded without the continued support of all of the CALLAS team members at Siemens and all of the OASIS team members at MCNC. Especially, we would like to thank Subhash Roy as the key designer of the register-transfer specifications of the QRS and FAN chips.

References


