Message from the Program Chairs
SiPhotonics 2015

With Exascale systems on the horizon, we will be ushering in an era with power and energy consumption as the primary concerns for scalable computing. Currently, the energy cost of moving data is becoming the dominant factor for the energy consumption, much greater than the computational energy cost. For instance, recent analysis shows that under 22 nm integration technologies data movement can represent about half of the power budget of a regular desktop processor and one fourth of the power budget of a server one. Furthermore, energy cost of on-chip data movements are expected to surpass soon (up to 10x) the cost of a 64-bit FLOP while off-chip accesses will even cost 100 to 1000 times more. At the same time, the evolution of challenging problems and advanced services need to support increased traffic intensity due to extreme-scale datasets and algorithm working-sets.

Photonic interconnects, and specifically integrated photonics technology, are one of the most promising solutions to increase the energy efficiency of communication in a computer system. Advances in silicon photonics have enabled the integration of all the building blocks of optical interconnects inside silicon chips (e.g.: lasers, modulators, waveguides, photodetectors). This disruptive technology can open new solutions to the problems of fast data transmission with low energy consumption in heterogeneous processor and memory architectures, which are crucial in the development of next generation computing systems.

However, current state-of-the-art research in this domain witnesses that these potential advantages can be fruitfully exploited only if a vertical cross-layer design approach is used aiming to find global optimum design points. This is mainly due to the very different features and constraints of the photonic technology for computing, compared to the well-known electronic counterpart. For example, end-to-end communication, circuit-switched nature and extreme fast propagation with almost distance-independent consumption are key features to exploit and to design around. Some integration problems of non-CMOS compatible modules pose challenges but wavelength-division multiplexing (WDM) inside the same physical waveguide allow bandwidth multiplication opportunities.

All these facets together contribute to the performance and consumption seen by the end user, and therefore there is a strong need for multidisciplinary approaches, studies and solutions, possibly crossing the traditional modular and hierarchical design, and shedding light into the paradigm shifts needed to operate successfully in this scenario.

Summarizing, silicon photonics can bring innovations and benefits into current and foreseeable computing systems directly, due to their intrinsic features, but also indirectly enabling the evolution towards architectures, runtime and resource management approaches that maximize the photonic raw technological opportunities and lead to more efficient overall designs, otherwise impossible.

The technical program of this year has two keynotes and five regular papers.

The regular papers have been grouped in two sessions. The first session, "From photonic network to architectural issues", focuses mainly on the interaction among optical networking and computer architecture issues.

The paper "High-Speed Optical Cache Memory as Single-Level Shared Cache in Chip-Multiprocessor architectures" from Maniotis et al., explores a big L1 cache architecture shared among all CMP cores and residing on a separate chip. The scheme is enabled by low-latency and high-bandwidth dedicated optical connection between cores and the cache-chip, which in turn benefits from a dedicated fast optical connection towards main memory chips. The paper witnesses an architectural opportunity exploitable only through the unique features of integrated photonic connection as wire delay issues would prevent such direction.

Then, in "On the Design of a Path-Setup Architecture for Exploiting Hybrid Photonic-Electronic NoCs", Fusella et al. underline the importance of path-setup design in hybrid photonic-electronic on-chip networks in order to fully exploit potential advantages of photonics and to reduce performance and consumption degradation risks. Various path-setup schemes are evaluated and a novel approach is proposed. Furthermore, the paper suggests that specific many-core architectures, and traffic features, can benefit from different path-setup procedures.
The second session, "From photonics technology to network issues", specifically addresses technological and on-chip networking topics. The paper "Partitioning Strategies of Wavelength-Routed Optical Networks-on-Chip for Laser Power Minimization" from Ortín Obón et al. explores network partitioning in wavelength-routed optical networks through wavelength assignment with two macro objectives: overall reduction of laser power and many-core partitioning to meet concurrent application needs. The core proposal leverages on the observation that the effect of physical on-chip distance can be dramatically reduced through fast optical propagation, enabling flexibility in assigning cores. Off-line exhaustive and on-line assignment algorithms are described and discussed.

Then, "Optimal Power Efficient Photonic SWMR Buses" by Eldhose and Sarangi, addresses the power consumption minimizing in SWMR rings and trees, proposing careful design through precise modeling of cascaded splitters. On the specific topic, the work provides a promising analytic methodology on how to design power efficient SWMR buses. Furthermore, the authors show that the linear-time proposed algorithm can be successfully exploited also at runtime using a hardware implementation that operates on configurable ratio splitters.

Lastly, Luo et al., in "Channel allocation protocol for reconfigurable Optical Network-on-Chip" present a new reservation protocol which is analyzed for the CHAMALEON adaptive optical NoC. The proposed approach aims at leveraging network partitioning, and the consequent wavelength reuse, within the same waveguide serving multiple endpoints. This can also support dynamic reconfiguration to adapt the same deployed resources to time-varying application needs. Both static and phase-related dynamic configurations are particularly suited for the stringent performance/energy needs of MPSoCs.

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