Making Medical Computation Affordable with VLSI

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"You ain't seen nothin yet"

Since the advent of the von Neumann digital computer roughly thirty years ago, the cost of computation has declined about 6 orders of magnitude. Uses of digital computers have grown at roughly the same rate so that we are now able to use computers in ways that would have been cost prohibited 30 - or even ten - or even a few years ago. Suitcase computers, easily affordable by individuals, have the power formerly found in "computer center" computers expected to serve the needs of entire universities just ten years ago.

While these rapid, evolutionary changes have had a profound impact on medical computation, with the advent of VLSI "you ain't seen nothin yet".

VLSI - what is it

VLSI stands for Very Large Scale Integration. The first von Neumann computers were made of vacuum tubes; transistors decreased the cost and increased the speed of computation by about 2 orders of magnitude each. Perhaps more importantly, the cost of ownership decreased by another 2 orders. Integrating several transistors onto a single silicon substrate, achieved during the 60s, further increased the speed and decreased the cost at least another order. Early integrated circuits had just a few logic gates but as the number progressed to 20-30, it became necessary to distinguish between small scale integration (SSI) and medium scale (MSI). Early microprocessors got above 100 gates opened up large scale integration (LSI). VLSI, in terms of gate count, is usually considered to be above 1000 or 10000 gates - but complexity rather than gate count is a better measure.

Several factors combine to allow such progress. Feature size, usually defined as the smallest transistor that can be made on the IC, decreases by a factor of 2 every two years while the size of the die increases by about 30%. Taken together we get about 5x the gates for a given die every two years.

Limits to Growth

The theoretical limit to feature size is about 125-250 angstroms, although Josephson junctions can be made at less than 100 angstroms. Current production processing allows feature sizes of about 2 microns with a few products appearing with feature sizes close to 1 micron. Consequently just on the basis of decreasing feature size increasing in complexities of 25-100 can still be obtained.

There is no known limit to die size. In fact, several laboratories are attempting "wafer scale" integration where the entire wafer (2-4 inches in diameter) is the die.

The current largest example of VLSI found in Hewlett-Packard's 32-bit microprocessor used in the 9000 desktop computer. It contains 450,000 transistors at a feature size under 2 micron with a die size just over .5 inches on a side. nMOS fabrication was used and a power dissipation of 4-7 watts is the result. Usually designers try to avoid, more than 1 watt/package; the HP-9000 has innovative packaging to dissipate this high heat production. Other technologies, particularly CMOS are being considered to reduce the power consumption.

Still another technique to solve the power dissipation
problem is to use active cooling. A fairly widely known secret research project is directed at using 2 inch wafers in wafer scale integration and "power hungry" ECL logic. In order to cool the logic the wafers will be mounted on metal blocks and freon will be circulated through the blocks to draw off the heat.

Progress in Peripherals

Just a few years ago it was widely predicted that rotating storage would disappear in favor of charge-coupled devices and magnetic bubbles. It now appears that neither of these technologies have made it through the technology window; to be cost effect CCDs and bubbles would have to be a tenth the price of RAM on a bit basis and are, in fact, ten times more expensive. In the case of bubbles there is little hope of spanning this hundred-fold gap; manufacturers seem to have given up on CCD memory devices because of severe processing problems. (Both technologies have special applications which will, no doubt, guarantee there continuing research and development.)

However, disk technology has, fortunately, progressed rapidly. Cost per bit continues to decline by a factor of four every two years. Access time has improved slightly along with reliability. Bit density has recently improved by 4-8 fold with vertical recording techniques which orients the magnetic domains vertical to the surface rather than horizontal. Mismatch in primary memory and disk speeds has been compensated in large measure simply by increasing the size of primary memory and using the extra memory as disk cache. Newer disk subsystems are using disk cache techniques integral to the disk controller and therefore enforcing optimal disk access algorithms such as the elevator algorithms.

A feeling for the state of the market is: 5 25 inch floppy format with 40 megabyte capacity have been introduced. Neither vertical recording or thin-film heads are used. Laboratory models of these drives have achieved 140 megabytes. State-of-art drives with both thin-film heads and vertical recording should produce this format at 300 megabyte quite easily.

In terms of archival storage, optical disks should appear on the commercial market within the next year. Although the early versions will have limited capacities, one can expect to see $10^{12}$ to $10^{15}$ bit capacities with 2-3 years and it is easy to conceive of even larger devices.

Portable, Desktop Computers by 1990

Portable, desktop computers will become a major market by 1990. What can we expect them to look like given the technology as it exists today and not counting on any innovations almost certain to occur -- a conservative estimate. It is relatively certain that these portables will be 32 bits (although 8 and 16 's will be with us for a long time). Memory sizes will be significantly more than a few megabytes and disks sizes will exceed 300 megabytes. Included will be both local-area network connections and at least 1200 baud (probably 4800 baud) modems. Gross processing power (raw CPU/memory speed) will be 2-3 greater than current super-minis and net or available processing power (power available to the user) should about 5 times greater than current super-minis. Assuming a sufficiently large market, almost certain to occur, the end-user cost should be on the order of $5000-10000.

The Real Problem -- Software

This paper has concentrated on hardware progress but it would be foolhardy not to mention the real problem of exploiting all of this potential. While computing power has increased by 6 orders of magnitude, nearly all of this improvement is due to hardware. At best software improvements contribute factors of 2-3. Much of improvements in software have been in the area of multi-programmed time-sharing operating systems and will have little use in personal computers. Progress in local area network operating systems has been slow as has been the work in distributed processing software of either tightly- or loosely-coupled systems. Perhaps even more importantly, however, is that programming languages continue to algebraic based (as opposed to, for example, command-and-control) and, given the increased complexity of the hardware, software systems require more effort to develop today than 20 years ago. Extrapolating the employment of programmers over the past twenty years indicates that we will need twice the current world's population as programmers just to fill our need in the year 2000. Obviously something must be
New Opportunities with Mead/Conway

New design methodologies pioneered mostly in Universities has made practical the direct implementation of digital algorithms as integrated circuits. Heavily dependent on Computer Aided Design (CAD), most major Universities have VLSI programs simultaneously investigating and improving CAD and educating a new generation of IC designers. Previous to Carver Mead and Lynn Conway's nearly single-handed effort to introduce the subject into University curriculum there were about 1500 IC designers in the United States. Since the introduction of Mead/Conway 3-4 years ago several times that number have been trained and industrial demand has risen even faster.

A significant feature of the Mead/Conway approach is that productivity is greatly increased. Previously the rule of thumb was "a million dollars and two years" for any new IC design. Recent microprocessors have cost on the order of 60 man-years and many millions of dollars for design. In contrast, a 32 bit microprocessor (RISC) was designed as a student exercise at Berkeley in less than a year at a relatively insignificant cost (hard to estimate). Utilizing MOSIS, a sophisticated software support system developed by DARPA and operating over ARPA net, a University designer can send a design to the Information Sciences Institute of USC and obtain a packaged IC usually in 1-2 months. Because of large number of designs flowing into MOSIS monthly fabrication runs are now done with about 50 projects being fabricated each month. Mead and Conway pioneered the Multi-Project Chip concept which allows many projects to share the cost of a single fabrication. Total fabrication costs for a nMOS run are about $20-25k and hence each of the 50 projects would cost about $500 in fabrication costs. Considering that PC board prototypes will often cost 5-10 this amount and require at least the same time for fabrication, MOSIS is at least as fast, considerably less expensive and results in an IC rather than a printed circuit board, i.e. a more desirable end-stage.

In the last year, simulation tools employed in the Mead/Conway approach have progressed to the point where a circuit now has better than a 90% chance of being functionally correct and operating at the specified speed on the first attempt at fabrication. While somewhat better than most industrial experience, there is every expectation that this will continue to improve.

New Approaches Afforded by VLSI

Several companies, notably INTEL, are introducing IC's to subsume major portions software systems in hardware VLSI devices. Kernels of operating systems, file systems, signal processors, graphics hardware, etc. which were formerly software, are being "embedded in hardware". Several advantages accrue from this approach: 1. Execution speed is greater, 2. Product installation time is decreased, 3. Version control is rigorously maintained, 4. Product cost may be lowered (although this is not clear yet) and 5. Proprietary interests are secure. Original design costs are significantly higher than a purely hardware approach but total life-cycle costs may be much lower. In any event, proprietary protection will probably dictate that we will see much more software embedded in hardware.

New non-von Neumann computer architectures are becoming quite attractive for a variety of computing functions. Very high speed string searching functions and matrix algebra operations have been demonstrated in in a general architecture referred to as systolic algorithms. A more general version of the CORDIC algorithms has been demonstrated and should yield operation speeds orders of magnitude faster than current computers for certain trigonometric problems occurring in signal processing.

Conclusions

VLSI will greatly increase the power and availability of digital computation to all uses of computers. We can expect to see portable 32 bit superminis in the $5-10k price range by the end of this decade. Software is a problem area but it is possible that software embedded in hardware will ease this problem. In any event, new non-von Neumann architectures will help to ease the software development costs at the same providing orders of magnitude increases in processing speed.