Welcome to the first of three sessions on Algorithms. This area of parallel and distributed computing is particularly interesting not only for the function and form of the algorithms considered, but also for their implementation within the parallel computing context. This session considers five papers with a broad range of application areas.

The first paper of this session, Wavelet Packet Zerotree Image Coding on Multicomputers by M. Feil and A. Uhl, considers the use of different types of multicomputer algorithms for advanced wavelet packet image coding. Specifically, the design of a parallel image coder composed of wavelet packet decomposition, based in conjunction with the best basis algorithm, followed by zerotree coding is presented. The experimental investigations obtained from a Siemens hpcLine cluster and Cray T3E concludes that the overall efficiency and scalability achieved does not justify the use of high end computing systems for this type of application. This is a particularly interesting finding which should provide useful information for all researchers with interests in this area.

The sequential sorting of large data sets in a parallel computing environment is the subject of the second paper of the session, The Effect of Local Sort on Parallel Sorting Algorithms by D. Jiménez-González, J.J. Navarro and J-L. Larriba-Pey. A new sequential sorting algorithm, Sequential Counting Split Radix (SCS-Radix) sort is proposed and evaluated in the context of the parallel computing platforms of a SGI Origin 2000 and an IBM SP2. Comparisons are made with other sorting algorithms, Radix sort and Quick sort in the same parallel context. It is demonstrated that the use of SCS-Radix makes the sorting operation insensitive to both skewed data distributions and partially sorted data sets, as well as achieving a significant reduction in sorting time.

Recent improvements in technology now allow multiprocessor designers to integrate components such as the memory controller and network interface inside the processor chip. The integration of a new three-level directory architecture is documented in the third paper of the session, Reducing the Latency of L2 Misses in Shared-Memory Multiprocessors through On-Chip Directory Integration by M.E. Acacio, J. González, J.M. Garcia and J. Duato. The work aims to reduce the long L2 miss latencies and the memory overhead that characterise cc-NUMA machines and limit their scalability. Execution-driven simulations of the proposed new architecture indicate a significant reduction in latencies which translate into reductions of up to 20% of execution times.

The fourth paper of the session, Parallel simulated annealing for the vehicle routing problem with time windows by Zbigniew J. Czech, presents a new approach to solving the vehicle routing problem. This is a problem in which a set of routes to a number of customers is minimised in terms of the number of vehicles used and the total distance travelled, assuming the vehicles originate and terminate at the depot. The algorithm proposed is concluded as being a novel and effective solution to bicriterion optimisation problems, performing particularly well to previously published benchmark sets.

A genetic algorithm designed for implementation in a parallel processing environment is reported in the final paper of the session, Parallel Single Front Genetic Algorithm for multiobjective optimization by F. de Toro, J. Ortega. The parallel single front genetic algorithm (PSFGA) is an elitist and pareto-based multiobject optimisation based on a subpopulation model. Experimental results on test cases are presented and indicate that the PSFGA performs better than the non-sorting genetic algorithm both in terms of convergence rate and size.