Special Session “Unorthodox Computing Architectures”

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The progress of hardware integration technology allows the cost-efficient implementation of innovative computing architectures which might constitute alternatives or add-ups to the current von Neumann computer architecture. Within this area, current research activities focus on issues like e.g.

- massively parallel processor architectures,
- architectures to support instruction level parallelism,
- data flow architectures,
- associative architectures,
- neural net architectures,
- biologically-inspired architectures.

This Special Session comprising four papers presents some recent progress in that area. The first paper, by B. Klauer, R. Moore, and K. Waldschmidt from University of Frankfurt describes the Self Distributing Associative Architecture SDAARC. This approach extends the paradigm of automatic distribution of data within distributed shared memories, to the automatic distribution of instruction sequences within distributed processor systems, thereby balancing the competing demands for parallelism on the one side, and for locality on the other side. It is shown how this is solved by a combination of static program analysis at compile time, to partition the dataflow graphs into coarser sub-units (so-called microthreads), and dynamic analysis at run time to map these microthreads to different available processors.

The second paper, by U. Rückert from University of Paderborn, presents some recently developed ultra large scale chips for realizing artificial neural networks features as e.g. neural associative memories and self-organizing maps. Subsequently, the third paper by M. Schmidt from Heinz-Nixdorf Institut, Paderborn and U. Rückert from University of Paderborn, in detail presents a novel approach for a neural associative memory, the Binary Neural Associative Memory BiNAM. Functionality and implementation of this architecture are described, and the tradeoff between hardware effort and the precision of results is discussed.

Finally, the fourth paper by K.-E. Grosspietsch from the German National Research Centre for Information Technology (GMD) and J. Büddefeld from the University of Applied Sciences Krefeld discusses a new approach for an associative processor system which is based on the integration of processing logic into a classical memory architecture. The merits of this architecture for implementing artificial neural networks are demonstrated, and a way to realize it by means of reconfigurable logic is shortly sketched.