Parallelism in Mainstream Enterprise Platforms of the Future

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Abstract

Today’s leading edge microprocessors feature over 200 million transistors. Moore’s Law continues to provide a doubling of the transistor density every two years. This has spawned several new changes in the features designed into commercially available microprocessors.

Intel’s Itanium® Processor Family features massive on-chip execution resources as evidenced by the 6 integer units, 3 branch units, 2 floating point multiply-add units, and 2 load and 2 store units in the recently released Itanium® 2 processor. Intel’s Xeon™ processor introduced simultaneous multi-threading (SMT) in a high volume microprocessor. IBM’s Power4* microprocessor represents the first “SMP-on-a-chip” design for high-end enterprise servers—two processors with Level 2 (L2) cache are incorporated on each chip. Future microprocessors will offer higher levels of multiprocessor capability on chip as the transistor density increases.

Computer manufacturers are incorporating these high-end microprocessors into large symmetric multiprocessing systems with 8, 16, 32 or even 64 processors. Another trend is the emergence of clustered commercially off the shelf (COTS) servers as credible supercomputing platforms.

These trends provide compiler writers and application developers a wide range of platforms for developing parallel applications ranging from instruction level parallelism (ILP) in high-end microprocessors, to tightly coupled thread level parallelism (TLP) and massive message oriented parallelism in large-scale clusters.

This talk will cover anticipated advances in semiconductor technology and relate those to trends in microprocessor design that will drive higher levels of parallelism in mainstream server platforms.

**Dr. Dileep Bhandarkar** is an IEEE Fellow, and a Distinguished Alumnus of the Indian Institute of Technology, Bombay, where he received his B. Tech in Electrical Engineering. He also has a M.S. and Ph.D. in Electrical Engineering from Carnegie Mellon University, and has done graduate work in Business Administration at the University of Dallas.

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Prior to joining Intel in 1975, he spent almost 18 years at Digital Equipment Corporation, where he managed processor and system architecture, and performance analysis work related to the VAX, Prism, MIPS, and Alpha architectures. He also worked at Texas Instruments for 4 years in their research labs in a variety of areas including magnetic bubble memories, charge coupled devices, fault tolerant memories, and computer architecture.

Dr. Bhandarkar holds 15 U.S. Patents and has published more than 30 technical papers in various journals and conference proceedings. He is also the author of a book titled Alpha Architecture and Implementations.