Abstract

With today manufacturing technology, it is not possible to eliminate all defects so that every manufactured unit is perfect. Instead, each manufactured unit must be tested so that defective parts are not shipped to a customer. In this situation, the test process consists in identifying defective circuits by applying test vectors in such a way that the presence of the defect can be observed on some circuit outputs.

Traditionally, test generation targets on fault models to produce tests that are expected to identify defects such as unintended shorts and opens. Test generation does not directly target defects for two main reasons. Firstly, many defects are not easy to analyze and no model exists to completely describe their behavior, thus making inconsistent test generation for these defects. Secondly, there can be a very large number of possible defects in a circuit. Since test generation and test application are limited by available resources such as memory and time, generating tests for all defects is unfeasible.

Consequently, a relatively small set of abstract defects, namely faults, is constructed and these faults are targeted to generate the tests. With this approach, the test quality relies on fortuitous detection of non-targeted defects. As the quality demands increase, the effectiveness of test generation without any defect consideration becomes questionable. High quality test generation requires a better knowledge of defect behavior.

As a matter of fact, the analysis of defect behavior is a quite difficult task. One of the main difficulties comes from the presence of random value parameters in the defects, preventing any prediction of the defect behavior. The mechanisms of defect appearance are obviously not controlled, resulting in electrical situations with unknown parameters. As a simple example, how to predict the voltage created by a short-circuit when the value of the short resistance is not known a priori. The classical assumptions such as zero-resistance short can no longer be used and a realistic analysis of defect behavior is required. A challenging but realistic model of defect behavior must now incorporate the random parameters. In the following different fault models for resistive bridging are revisited.

1. Classical Fault Models

Historically many fault models have been used to detect bridging defects, each new model generation trying to more precisely describe and represent the real defects.

In the early 80’s, the most used fault models were the wired-AND, wired-OR and Dominant models. In fact, these first purely ‘logic’ fault models did not consider any electrical parameter of the real bridging
defect! Obviously, it has been observed that detection of real defects was not very efficient when using these models.

2. Realistic Fault Models
Models have been progressively improved by considering the electrical parameters of the defect. For example, one can find in the literature the series of the so-called ‘Voting models’. In these models, it is considered that the defect creates an intermediate voltage on the shorted nodes. As a consequence, the objective of the voting model was to easily compute the intermediate voltage in an efficient way during fault simulation for example. Remember that a model must be easy to manipulate and handle by the test tools and consequently must ensure a reasonable CPU time when implemented in the test tools. These models usually qualified as ‘Realistic fault models’ have been used in fault simulation and ATPG for years.

3. Realistic Defect Model
The most recent models take the bridge resistance into account. For this new model, the objective is no longer the computation of the intermediate voltages resulting from the bridging defect. Indeed, the resistance of the bridge is a parameter of the defect that cannot be predicted. Now, the voltage value of the shorted nodes depends on the random resistance of the bridge. Rather the basic concept of this new model is the evaluation of the range of detectable resistance as illustrated below.

In the presence of a zero bridge resistance, both nets have the same voltage value and the circuit exhibits faulty logic behaviour. However, as the bridge resistance increases, the voltage of the bridged nets gets closer to the defect free value so that for high resistance values, the circuit operates properly. In this way, there is a critical resistance value \( RC \) above which the circuit does not show faulty logic behaviour. This behaviour is illustrated in the Figure below. Suppose that the bridge is excited in such a way that \( VA \) is set to logic 1 in the defect free case, whereas \( VB \) is set to logic 0. The plot in the Figure represents the voltage of the bridged nets as a function of the bridge resistance. For a zero bridge resistance, both \( VA \) and \( VB \) have the same value. However, as \( Rb \) increases, \( VA \) increases and \( VB \) decreases, to the point that \( Rb \) is so high that \( VA \) is properly interpreted by \( NAND3 (RC(NAND3)) \), and for a higher resistance \( VB \) is also properly interpreted by \( NAND4 (RC(NAND4)) \). Therefore,

- When \( Rb < RC(NAND3) \), logic errors are propagated through both \( NAND3 \) and \( NAND4 \).
- When \( RC(NAND3) < Rb < RC(NAND4) \), logic errors are propagated through \( NAND4 \).
- When \( Rb > RC(NAND4) \), the circuit does not show faulty logic behaviour.

For a given resistive bridging defect, the proposed model allow to easily compute during fault simulation, the different critical resistances \( RC(NAND3), RC(NAND4) \) which in fact define the range of detectable resistance associated to the defect. This information is used during fault simulation and ATPG to guide the test generation process and to evaluate some quality metrics of the test vectors.

4. Conclusion
The presentation will give details on the definition of these new defect models as well as implementation in fault simulation and ATPG tools. Information may also be found in the references given below.
Biography

In 1986, Michel Renovell joined the Laboratory of Computer Science, Automation and Microelectronics of Montpellier where he is a researcher funded by the French National Council for Scientific Research (CNRS). From 1995 to 2005, he served as head of the Microelectronics teams at LIRMM. Since 2006, he is Scientific Advisor for the National CNRS headquarter managing more than 300 labs in France. He is also Director of the ‘French National Network on SOC/SiP Design & Test’. He is a member of the editorial board of JETTA, the editorial board of IEEE Design & Test and the editorial board of the VLSI Journal. Michel was general chair and program chair of many conferences, he has published over 150 international papers and has received several best paper awards. His research interests include: Fault modeling, Analog testing and FPGA testing.